

10/20/07

FIG. 1

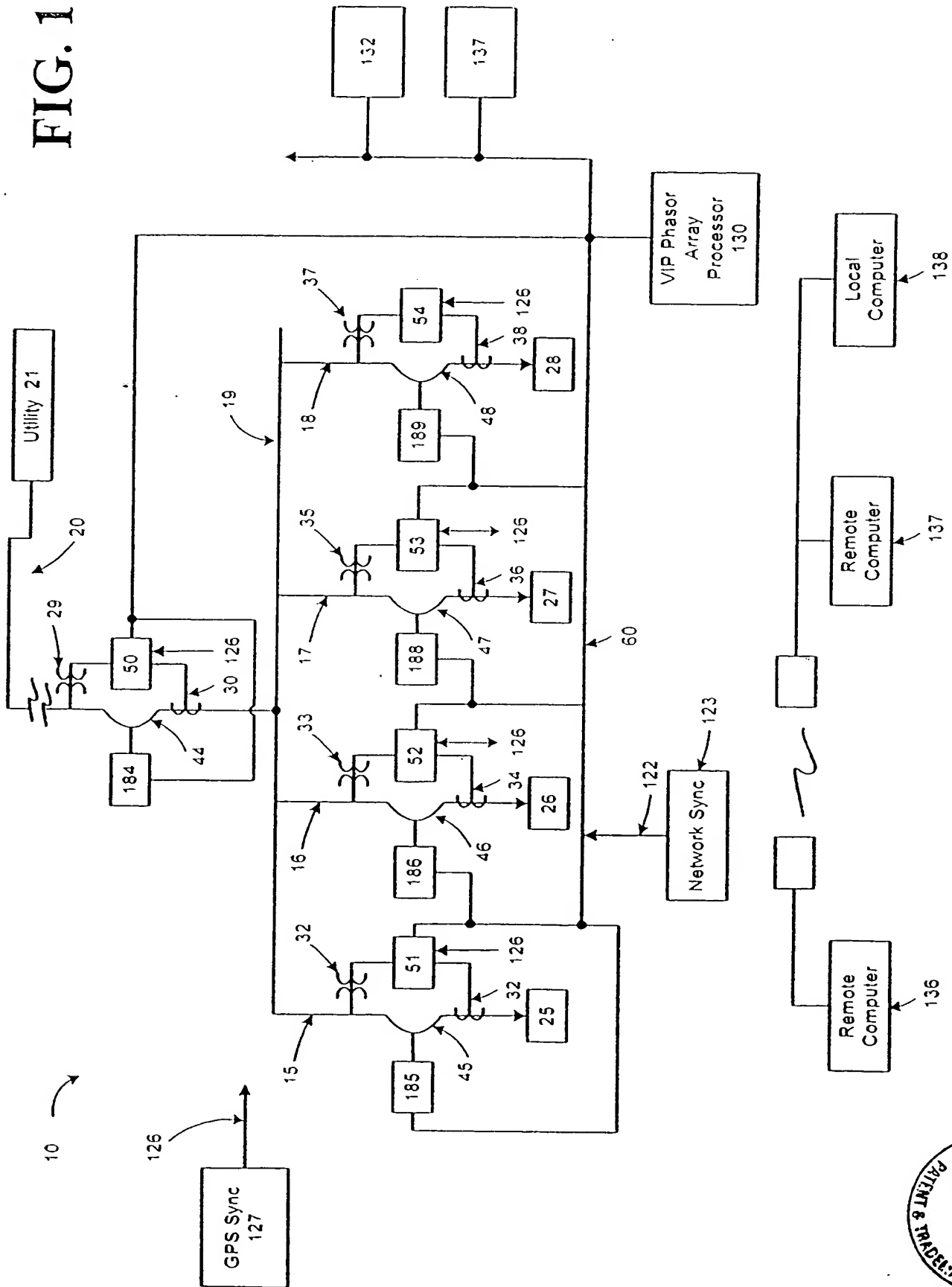
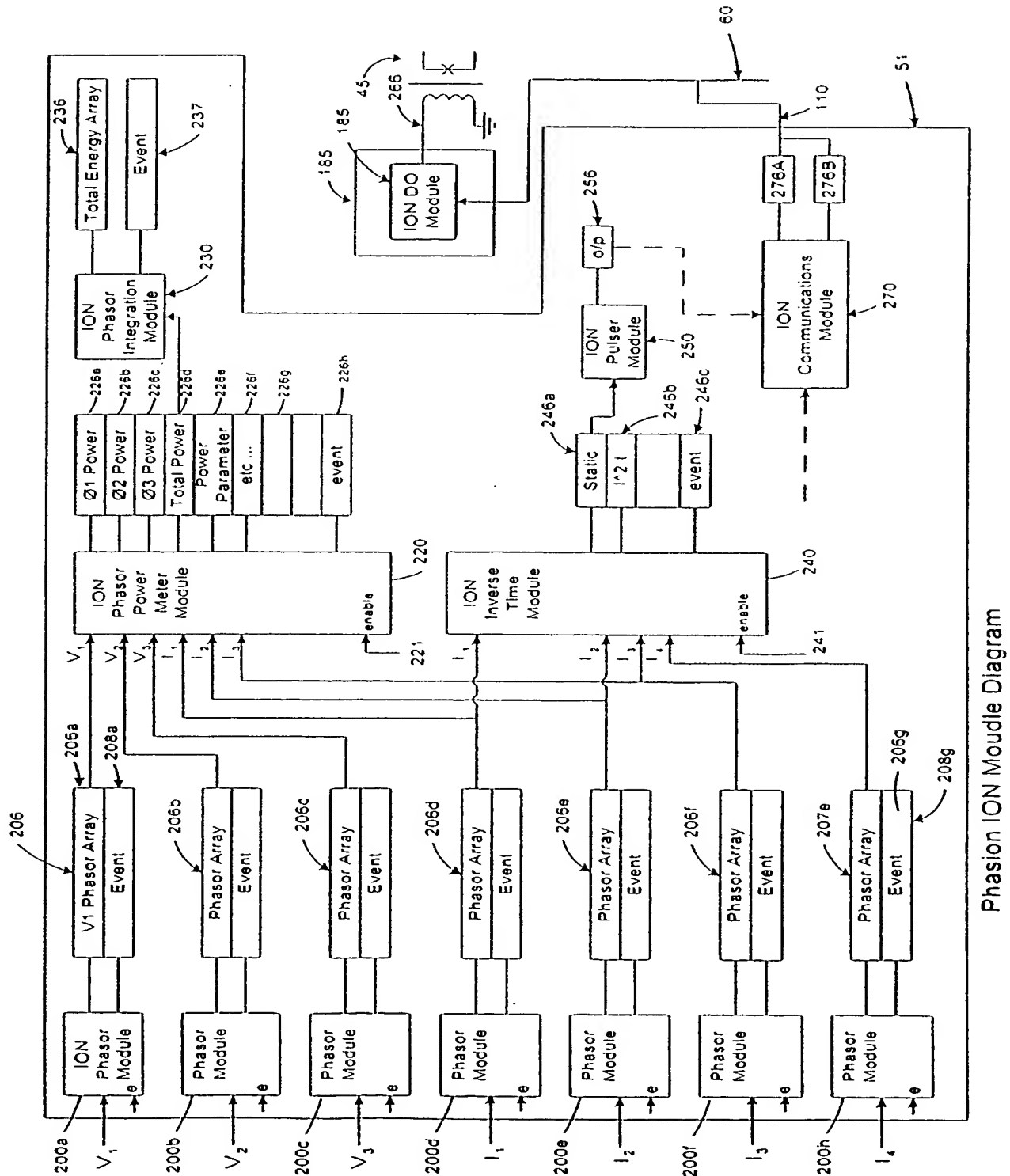
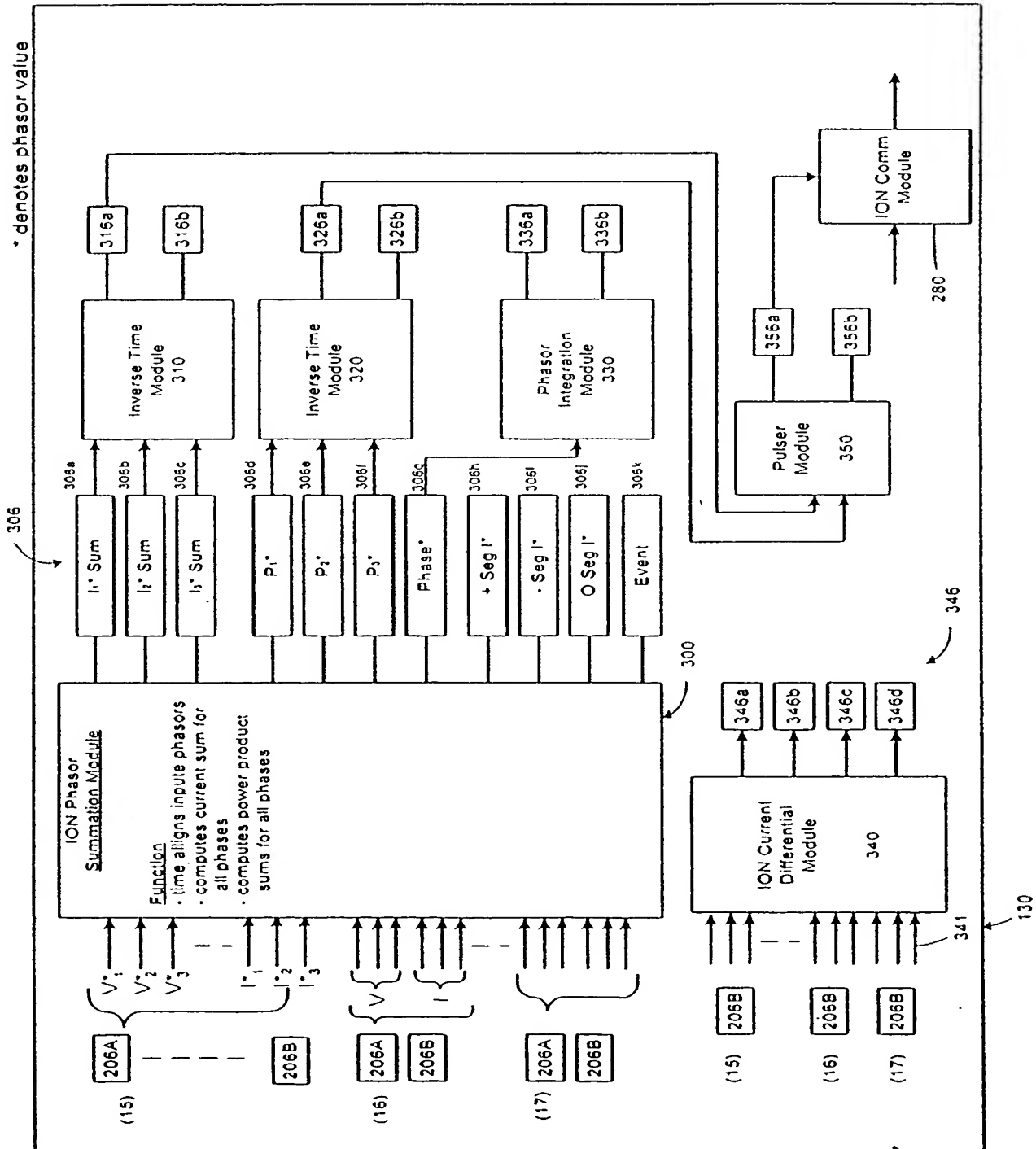




FIG. 3







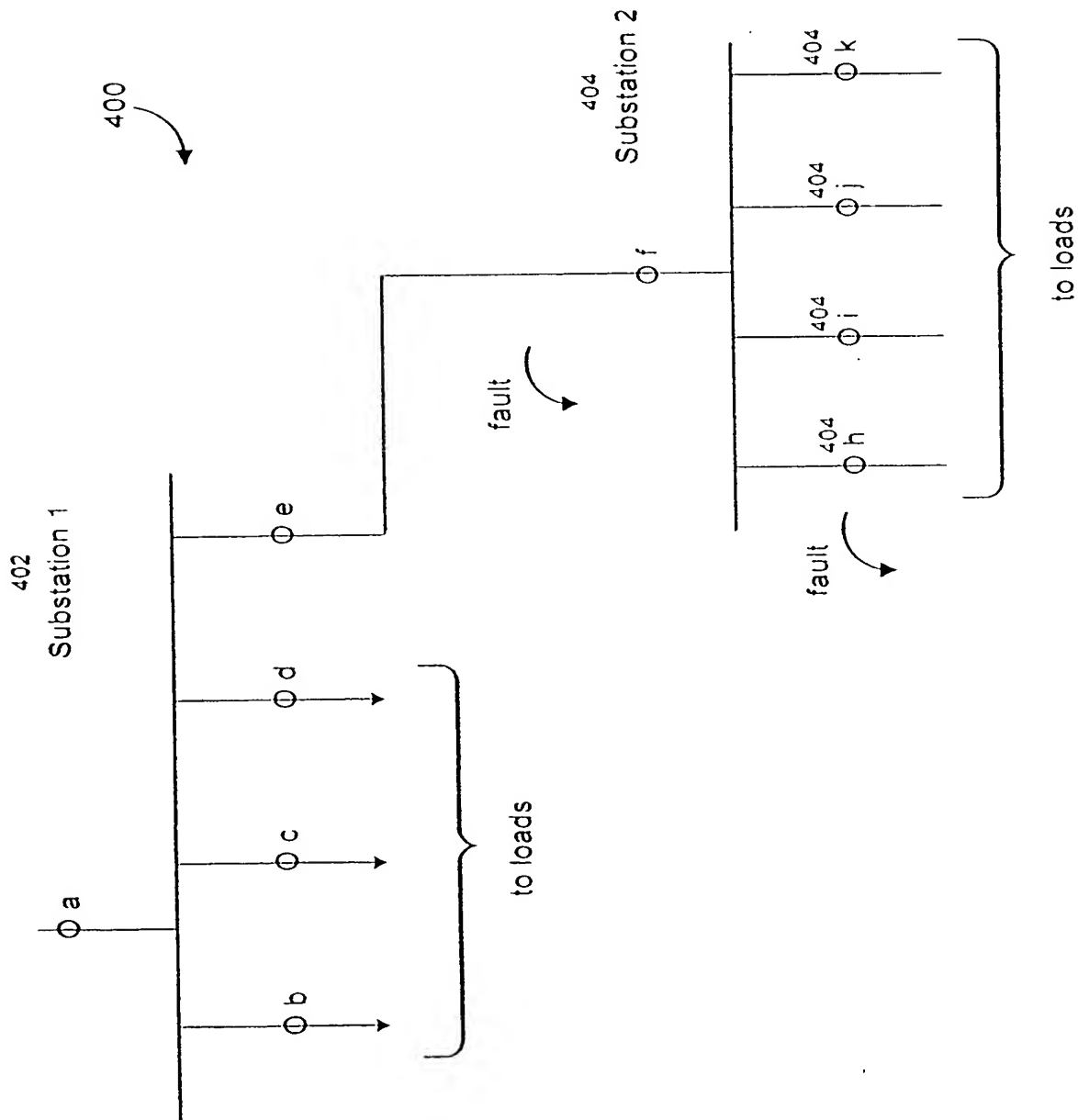


FIG. 5

FIG. 6

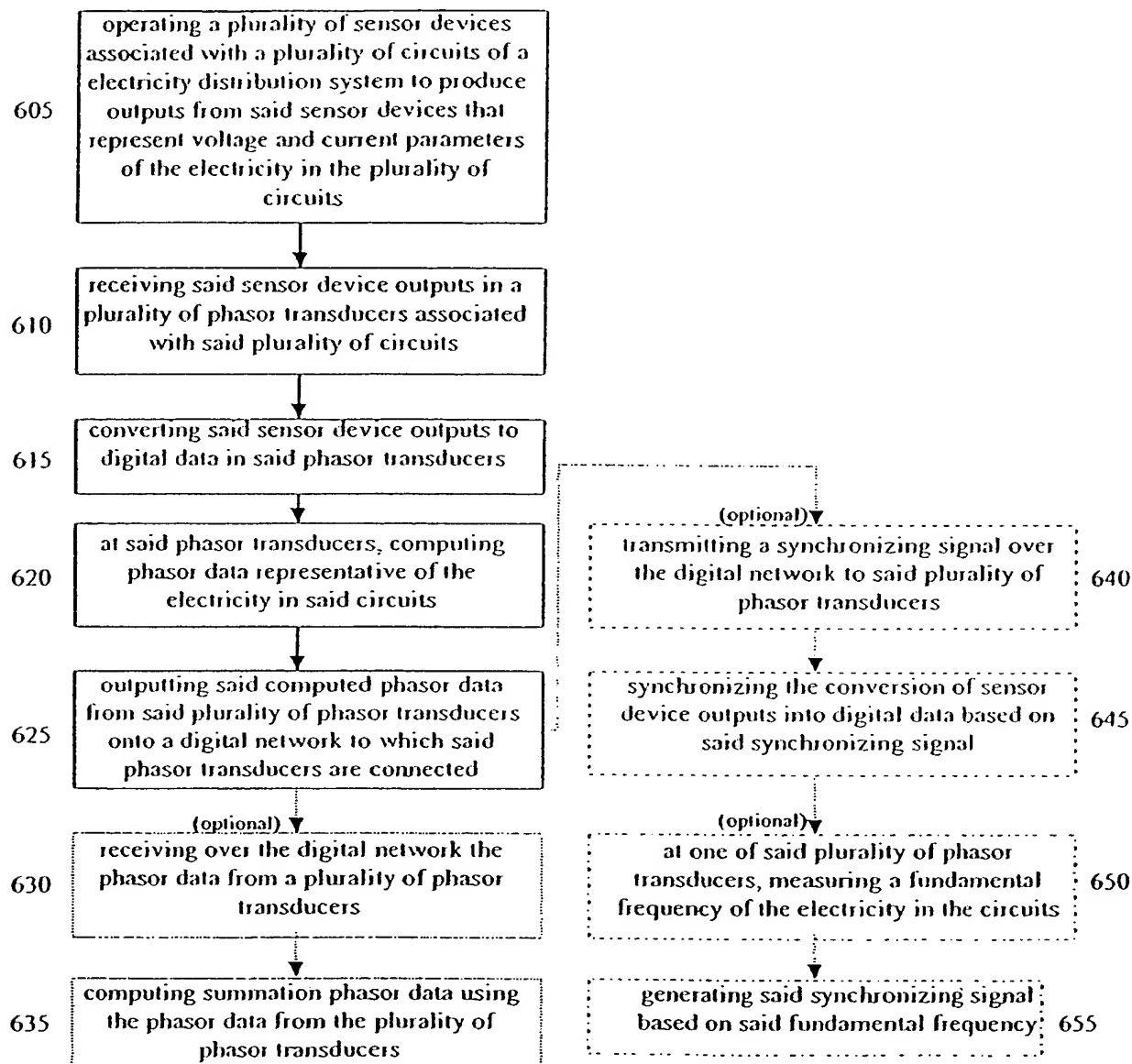


FIG. 7

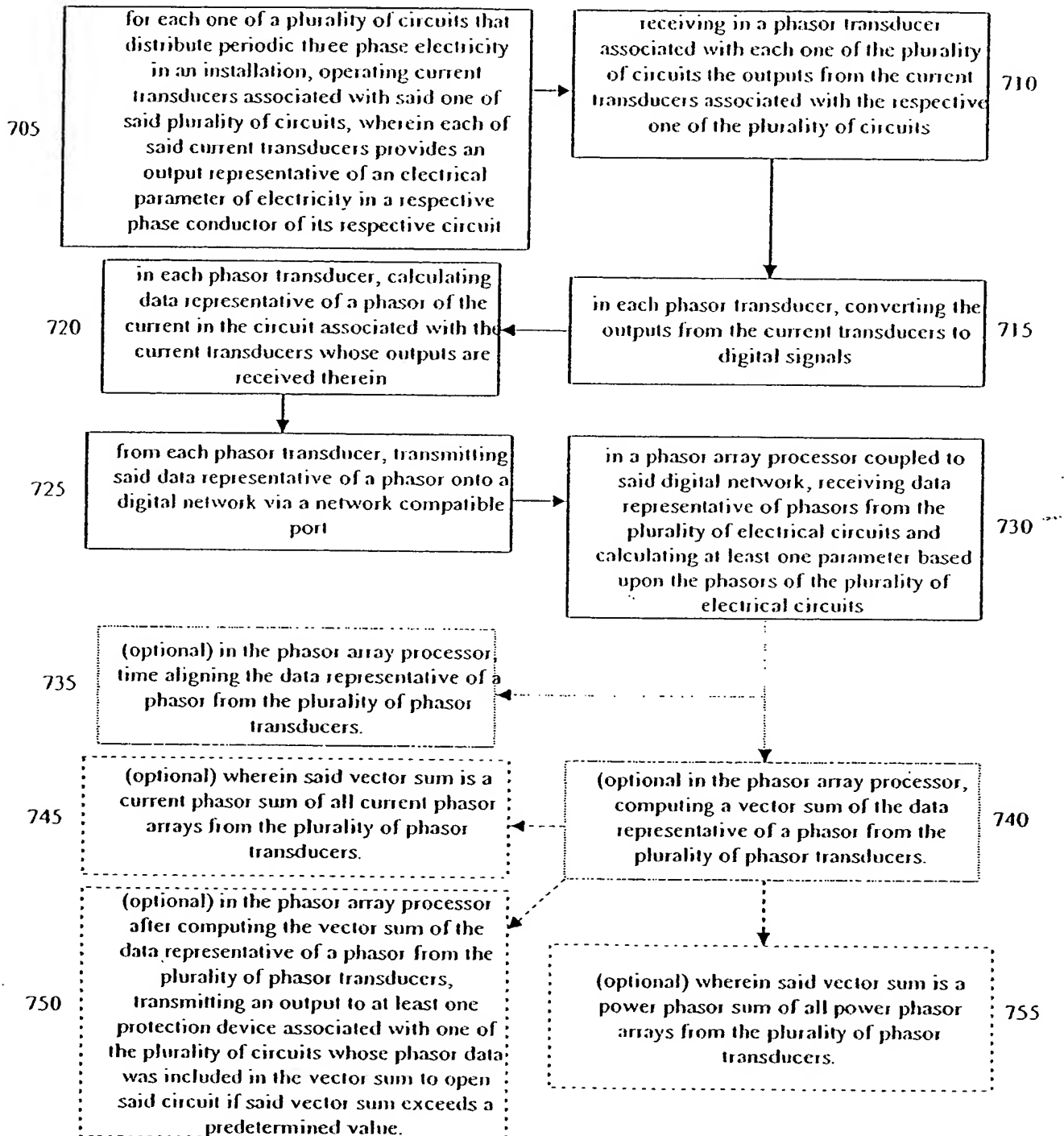


FIG. 8

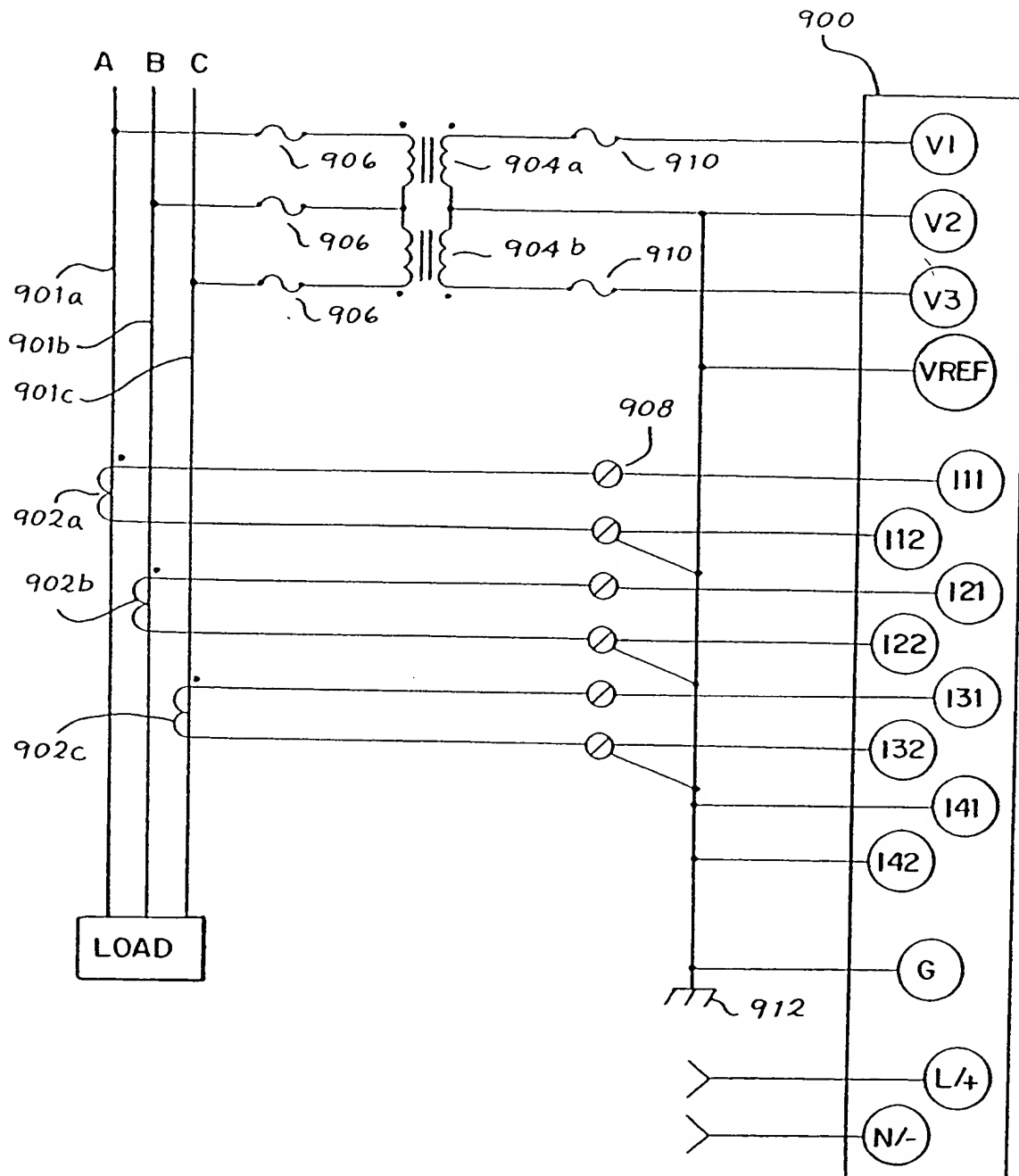


FIG. 9

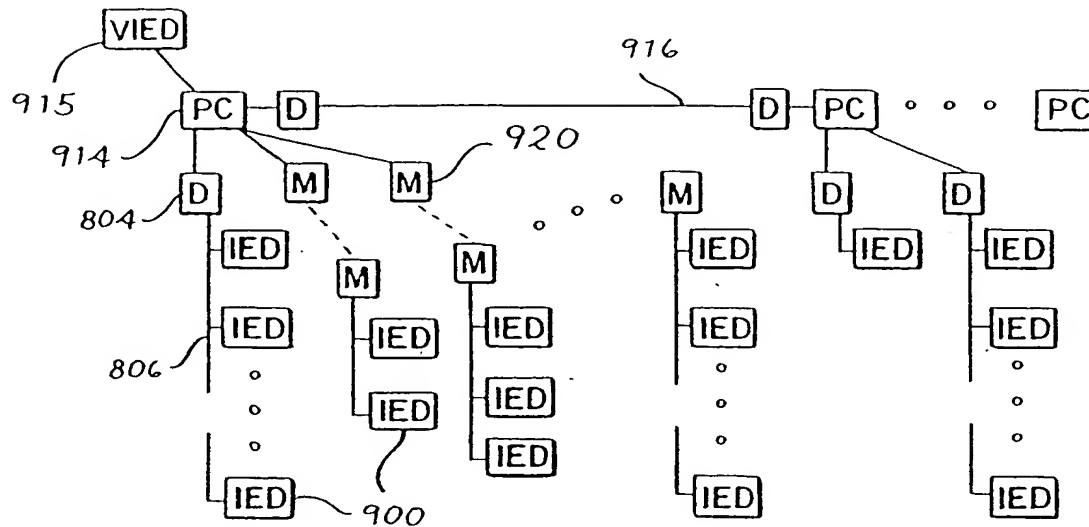


FIG. 11

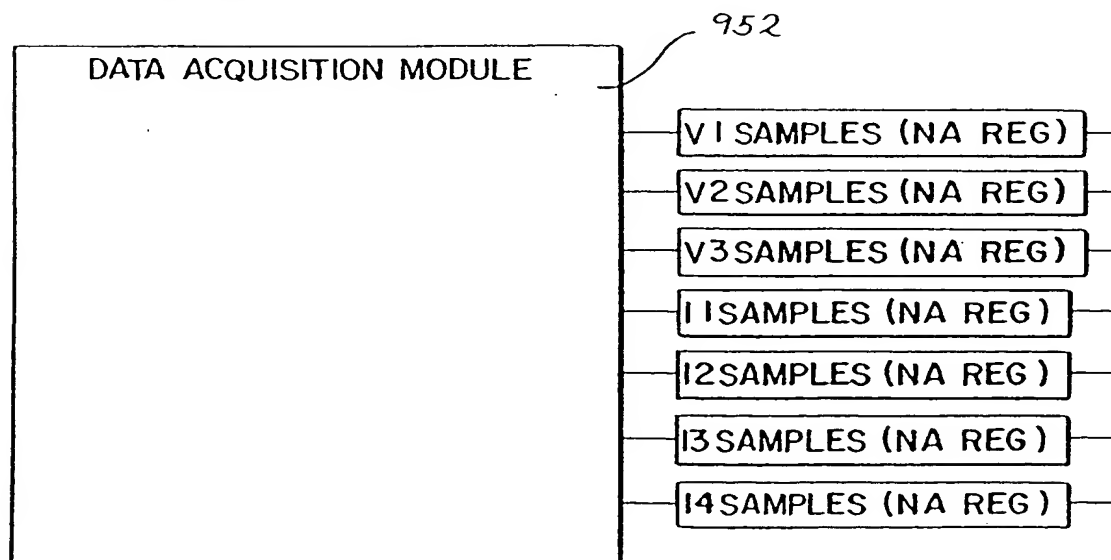
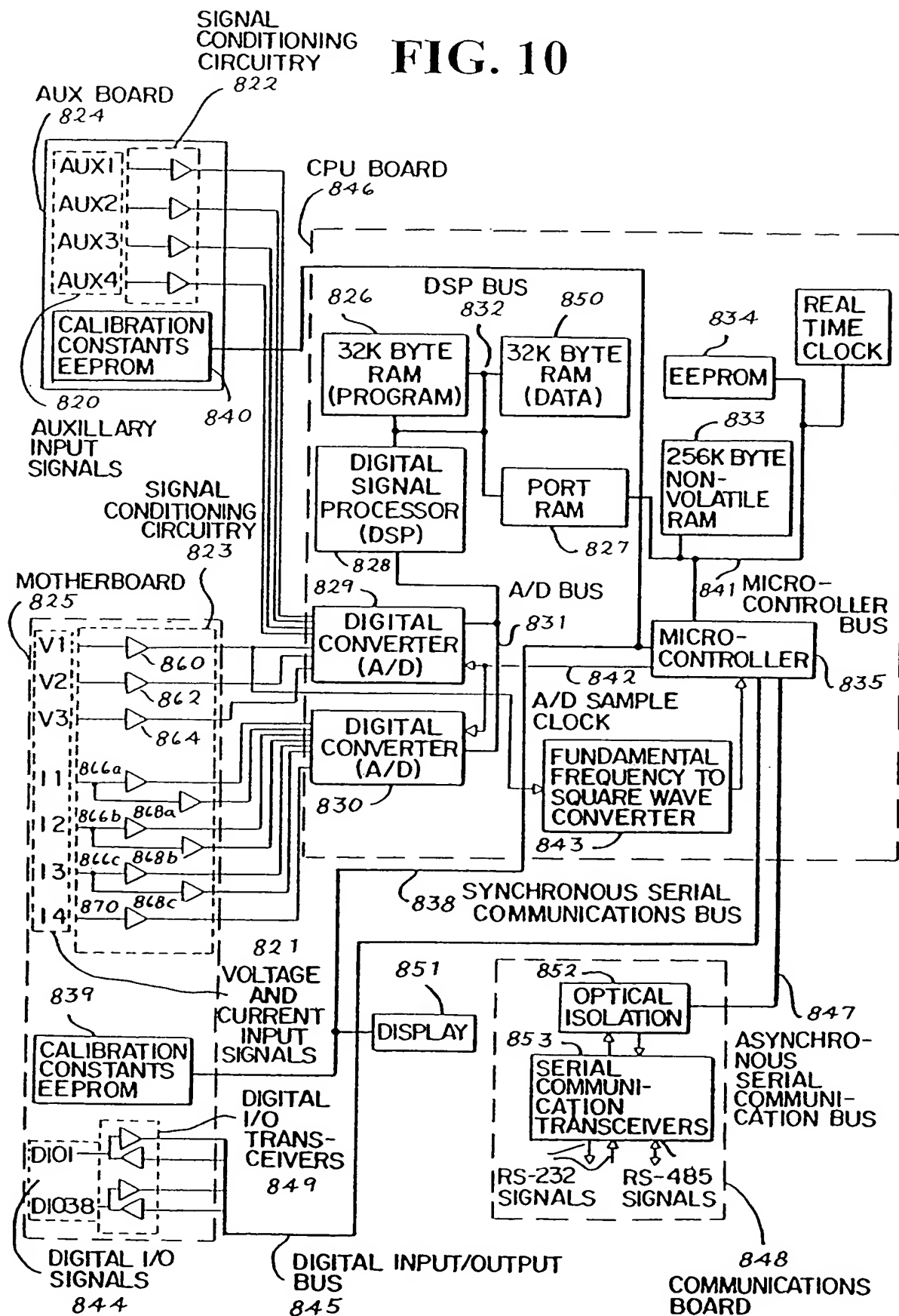


FIG. 10



DATA ACQUISITION  
MODULE  
OPERATION (CLIENT  
PORTION)

FIG. 11A

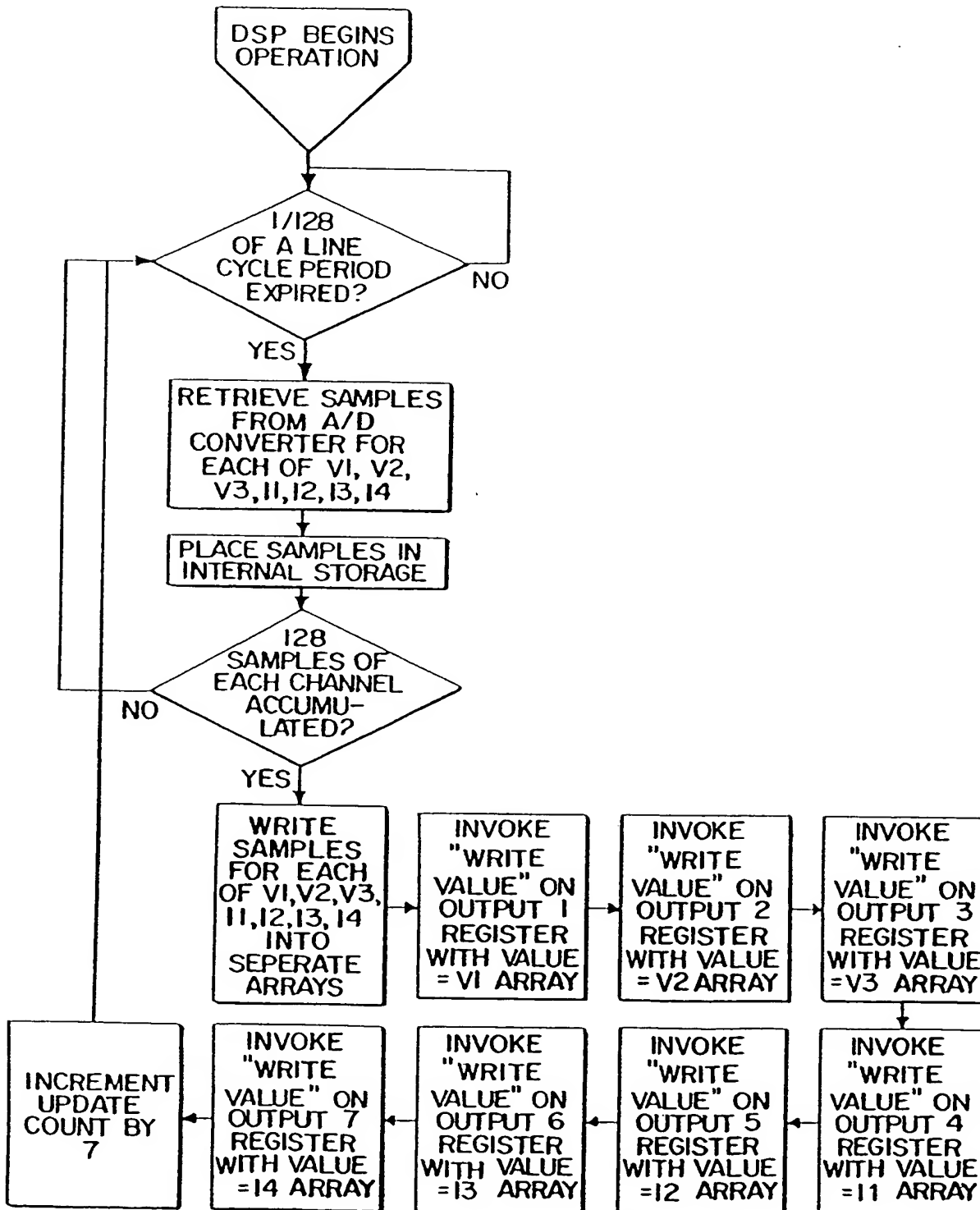
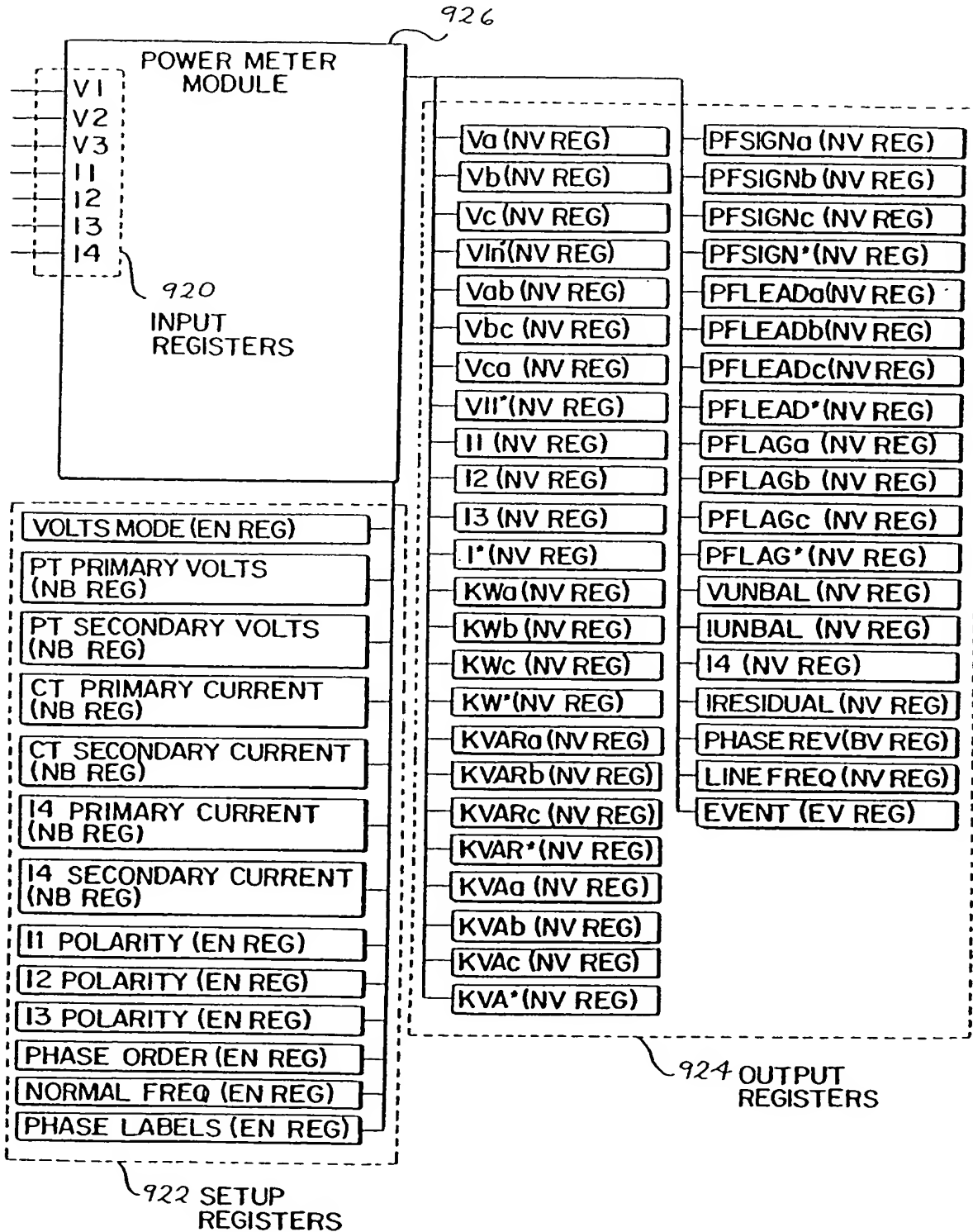


FIG. 12





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FIG. 12A

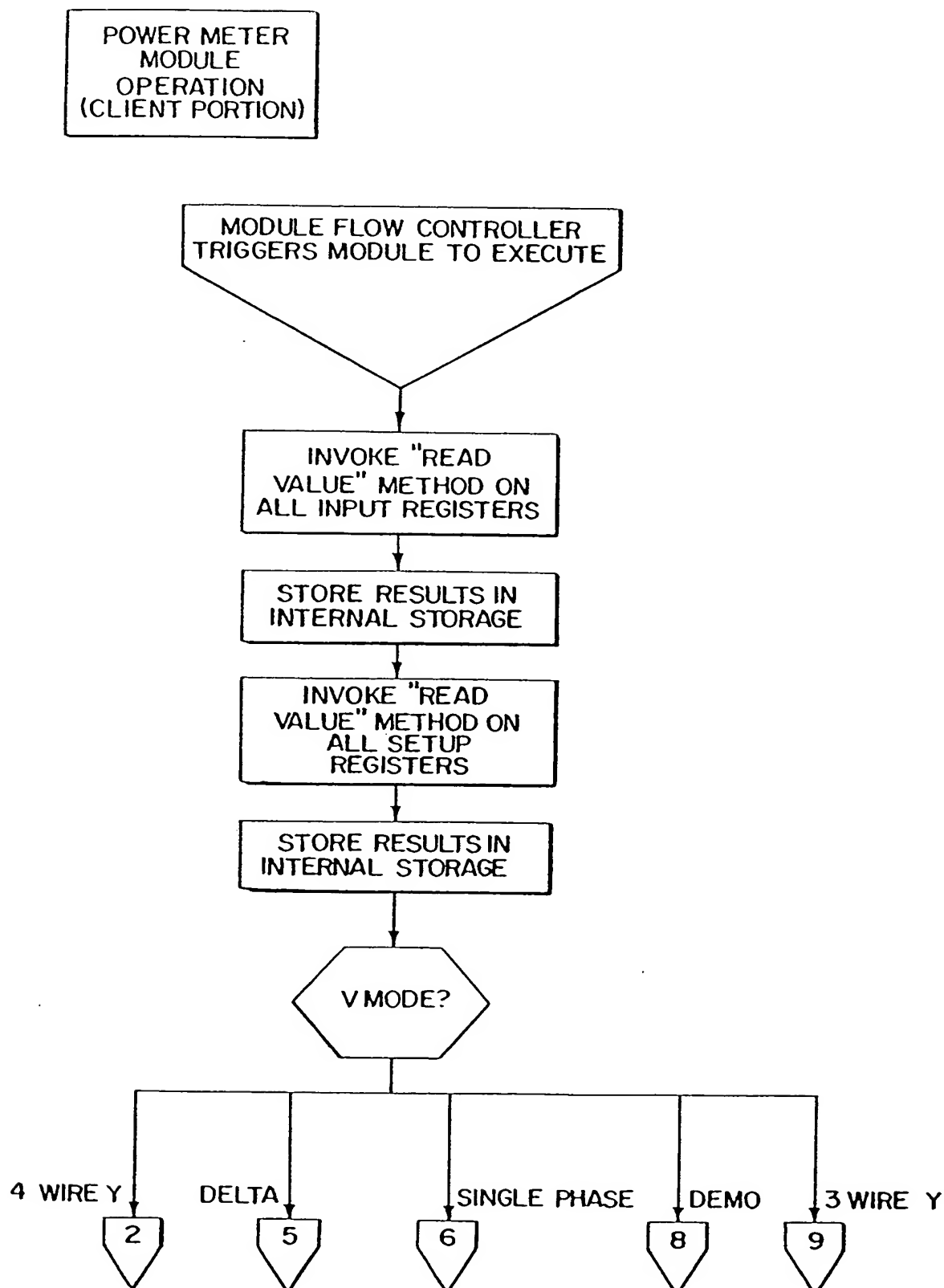




FIG. 12B

FIG. 12C

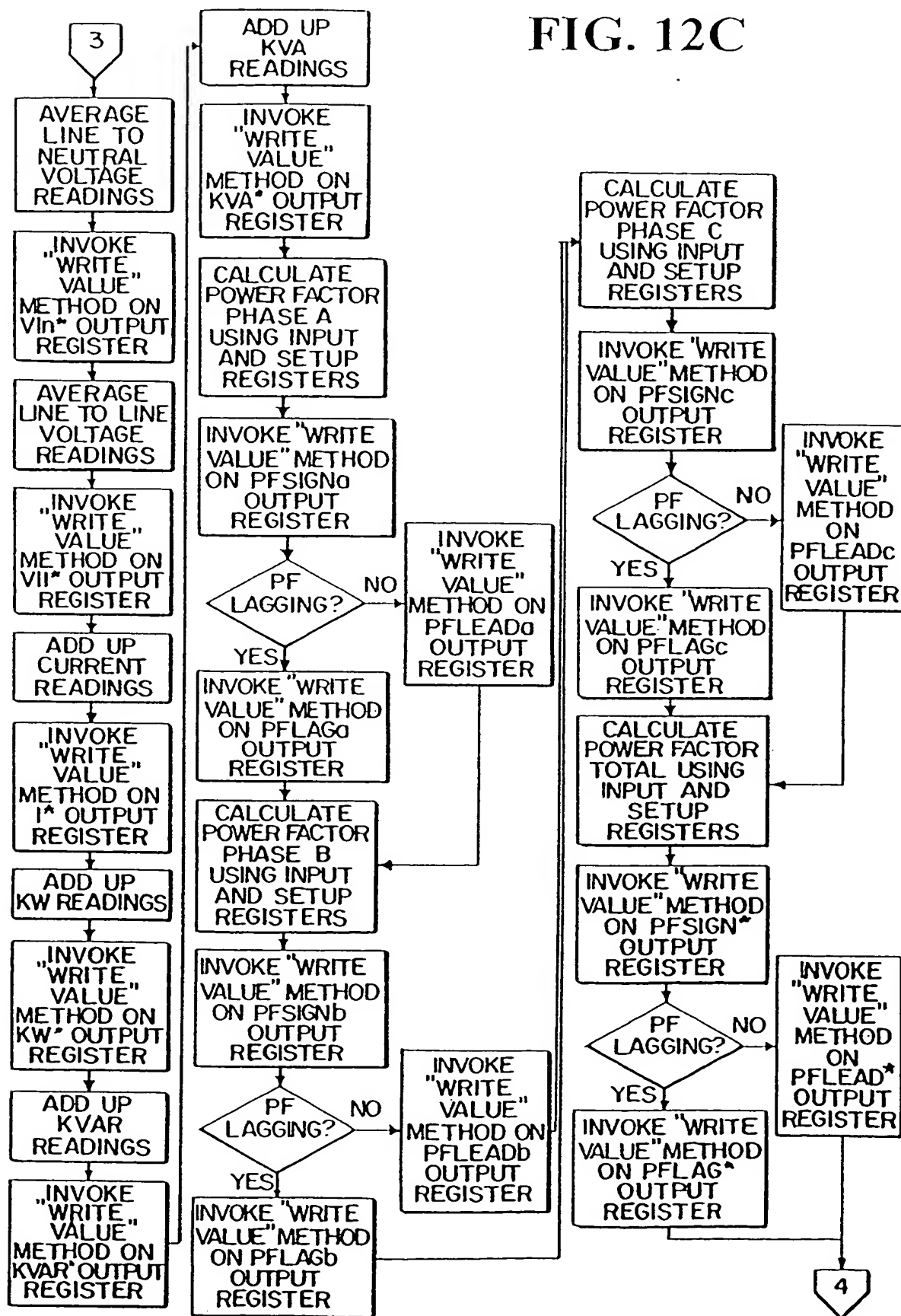


FIG. 12D

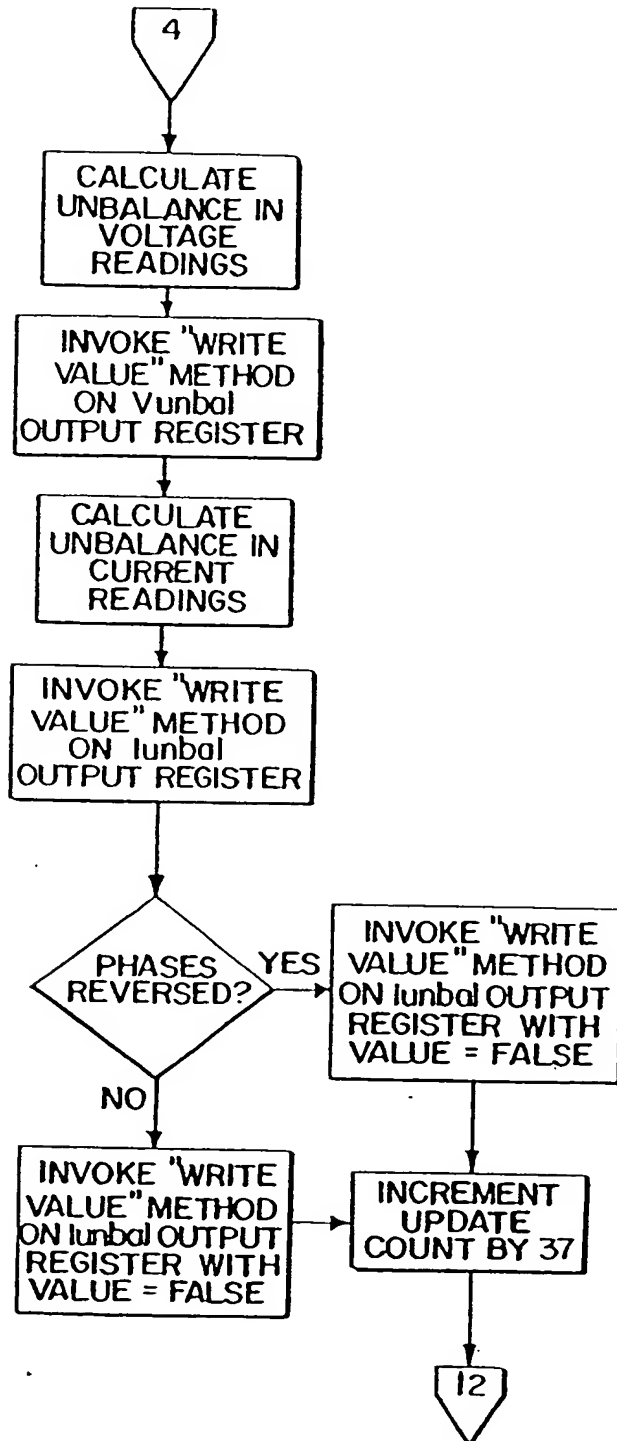


FIG. 12H

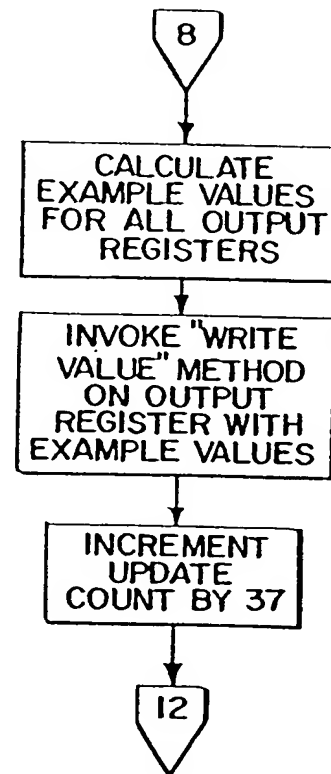


FIG. 12E

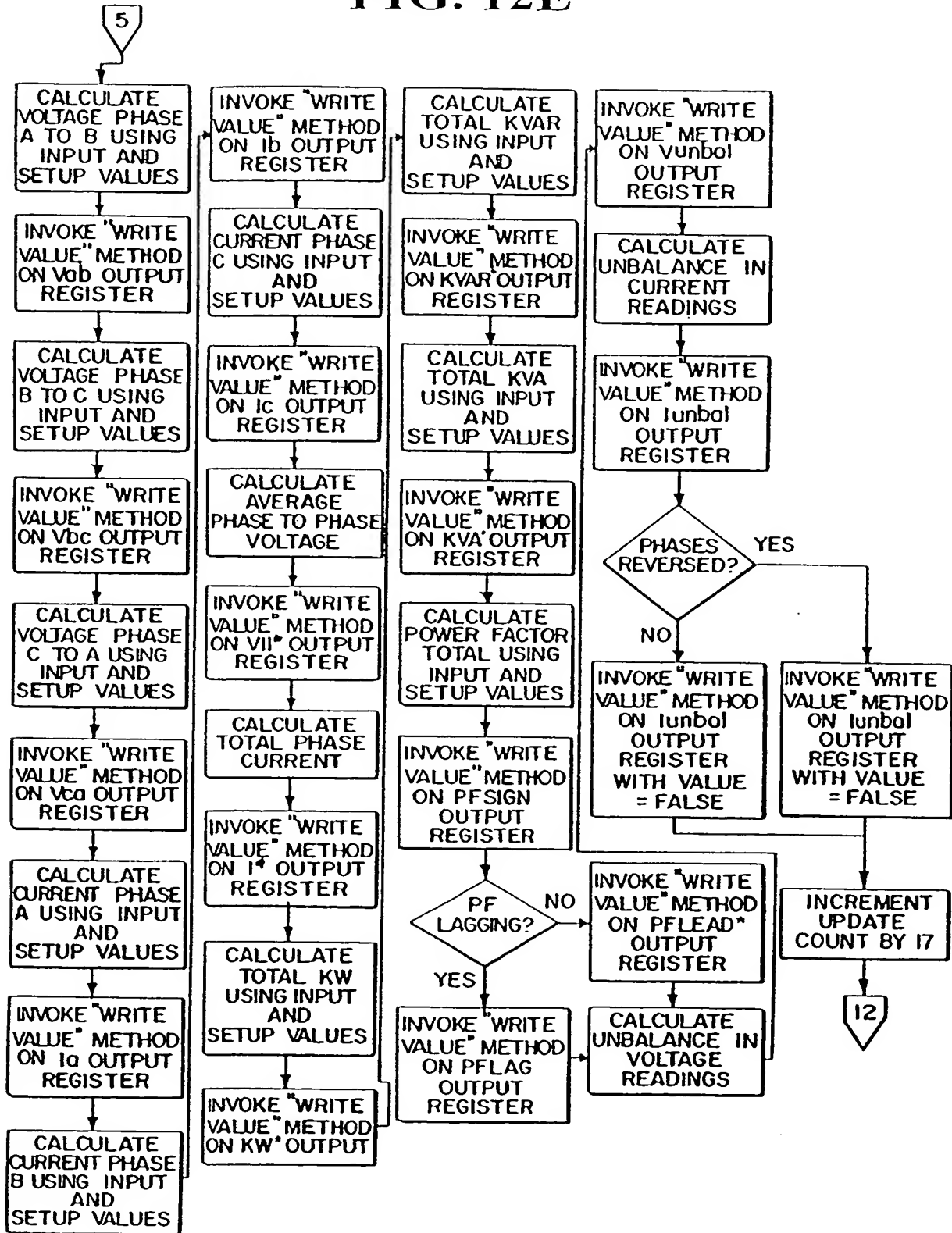


FIG. 12F

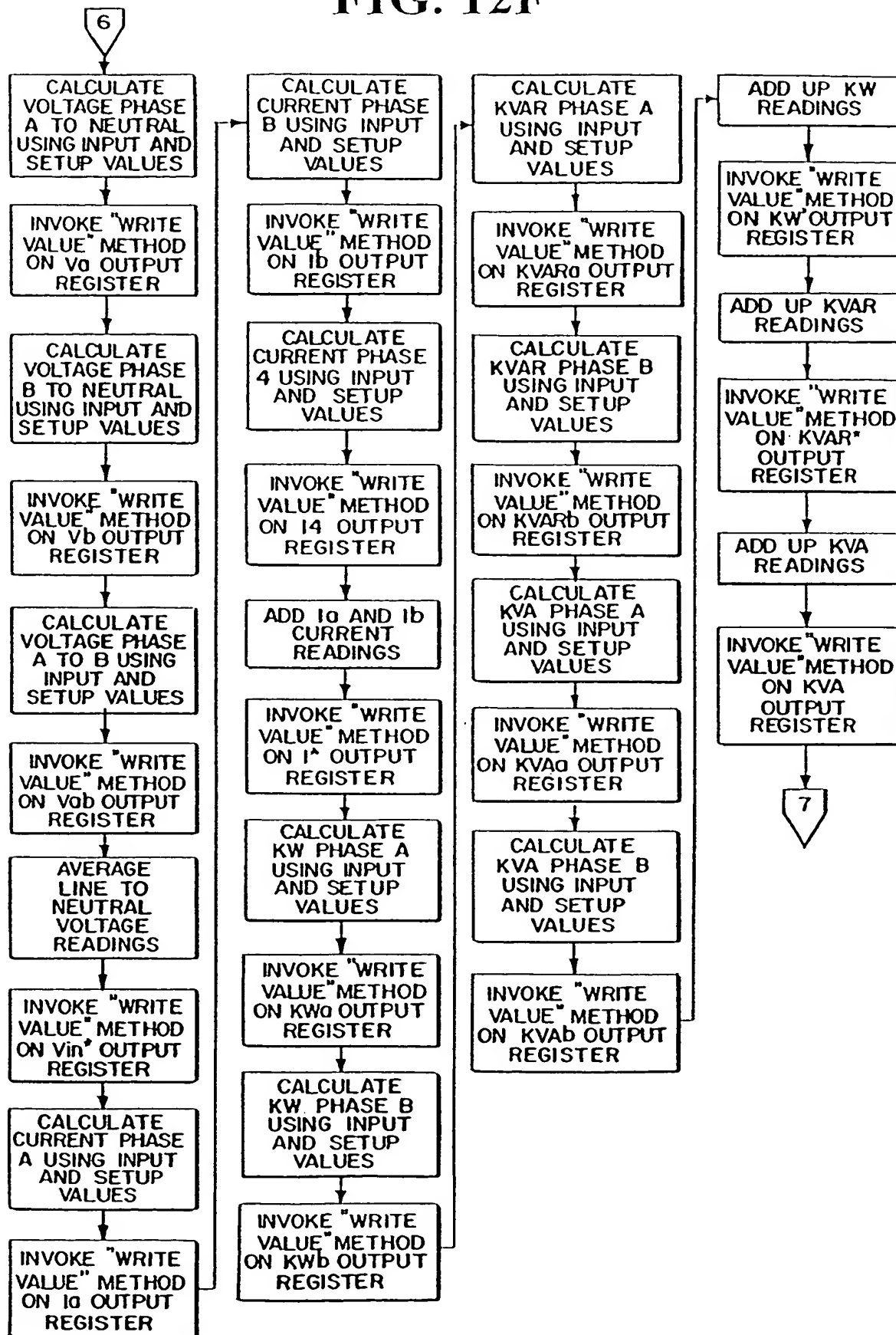
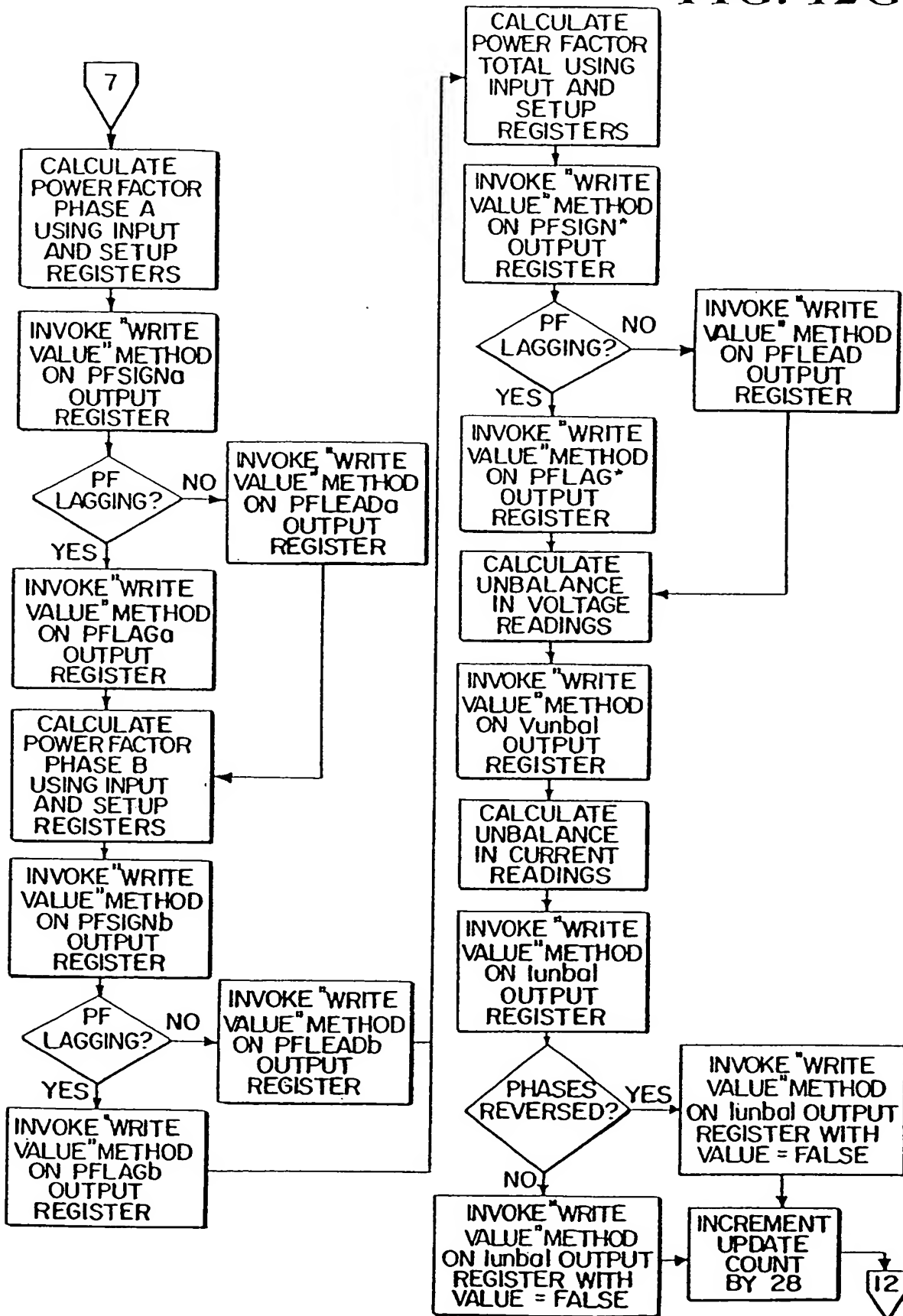


FIG. 12G



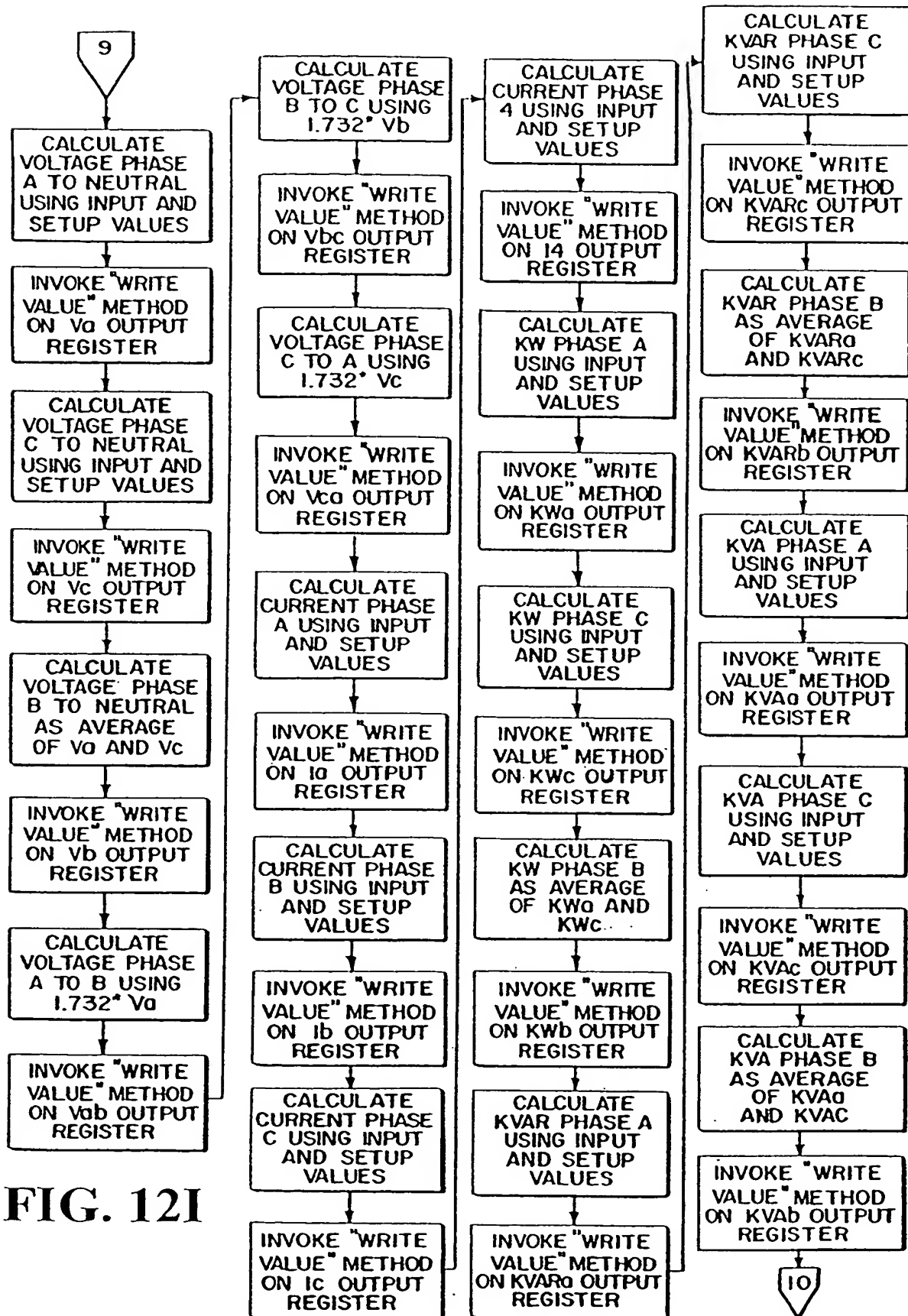


FIG. 121



FIG. 12J

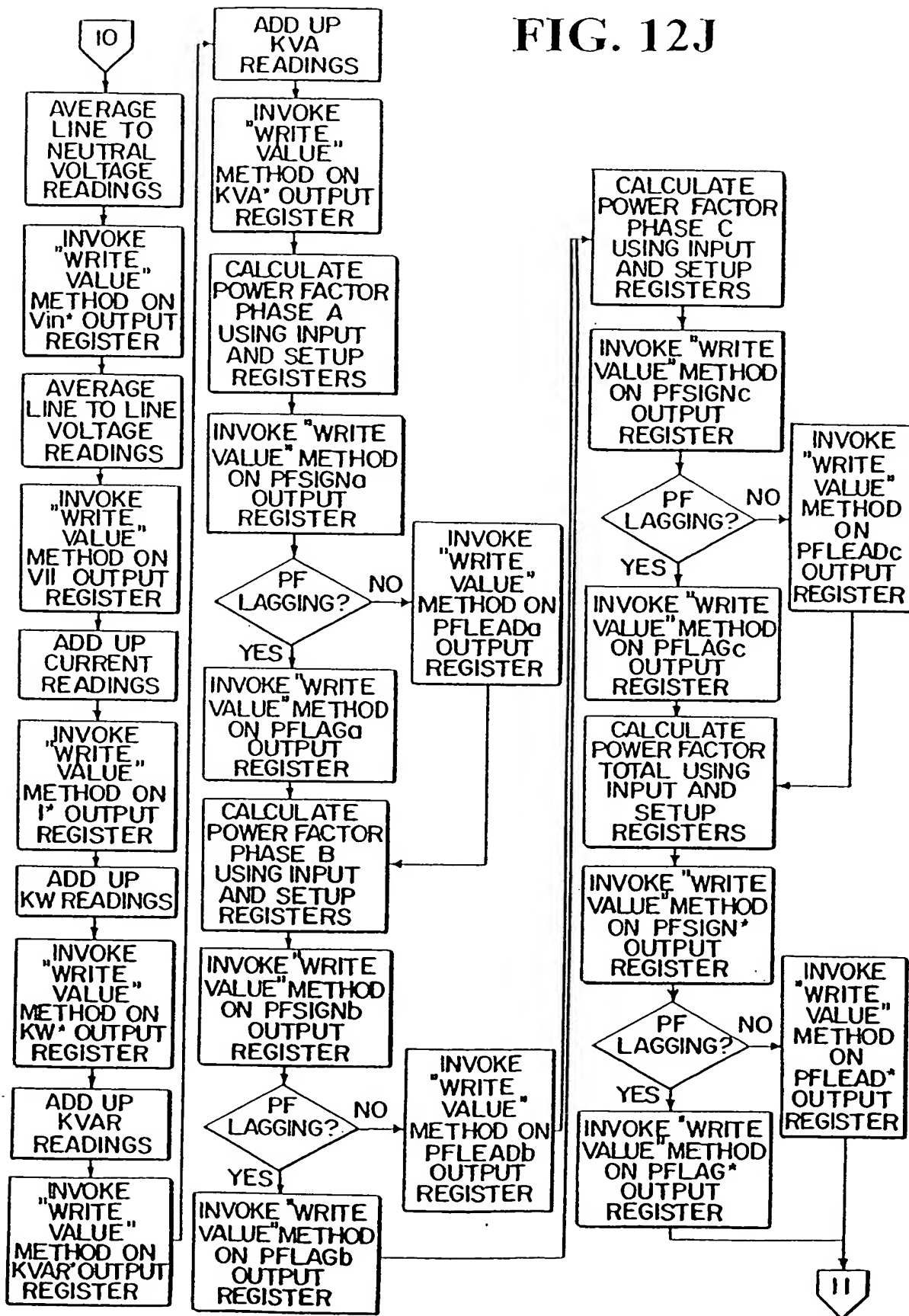


FIG. 12K

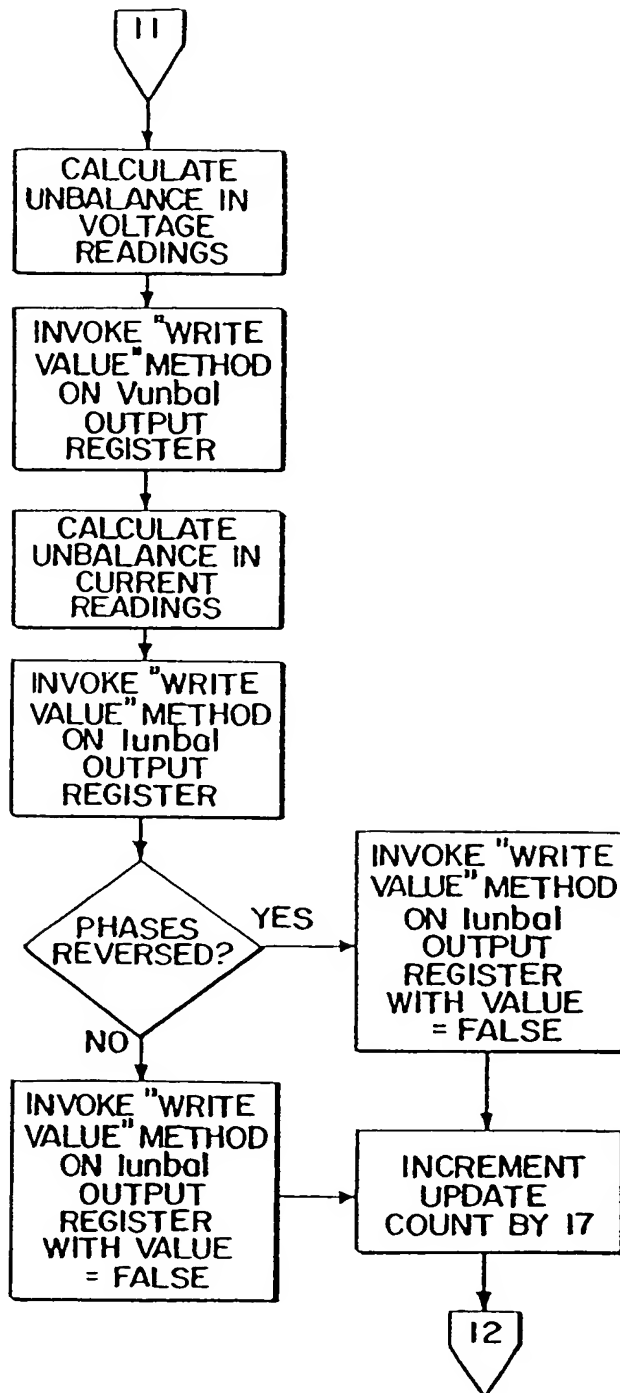


FIG. 12L

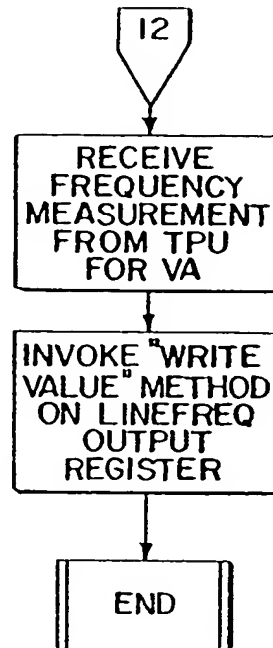


FIG. 13

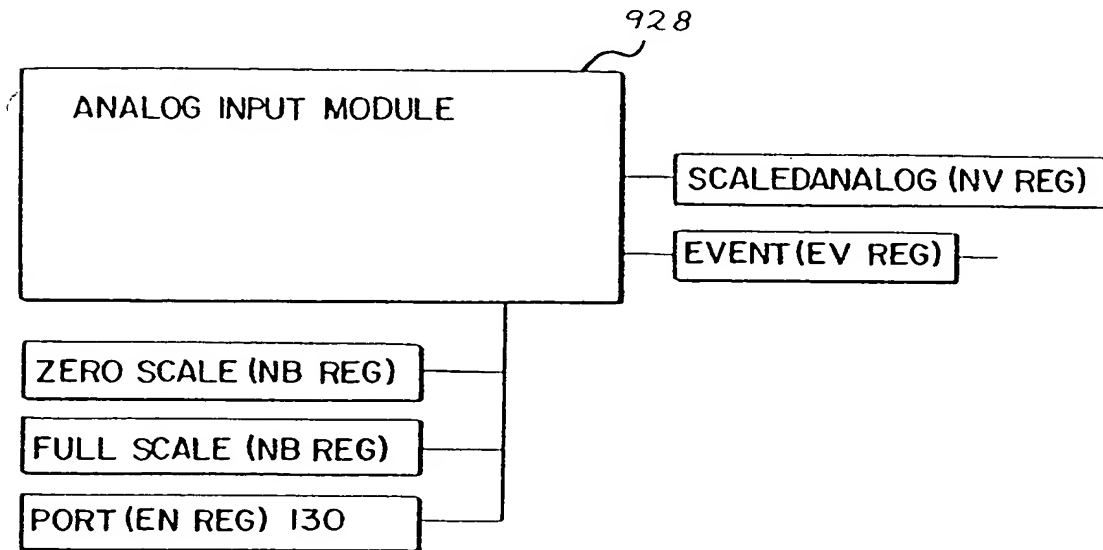


FIG. 14

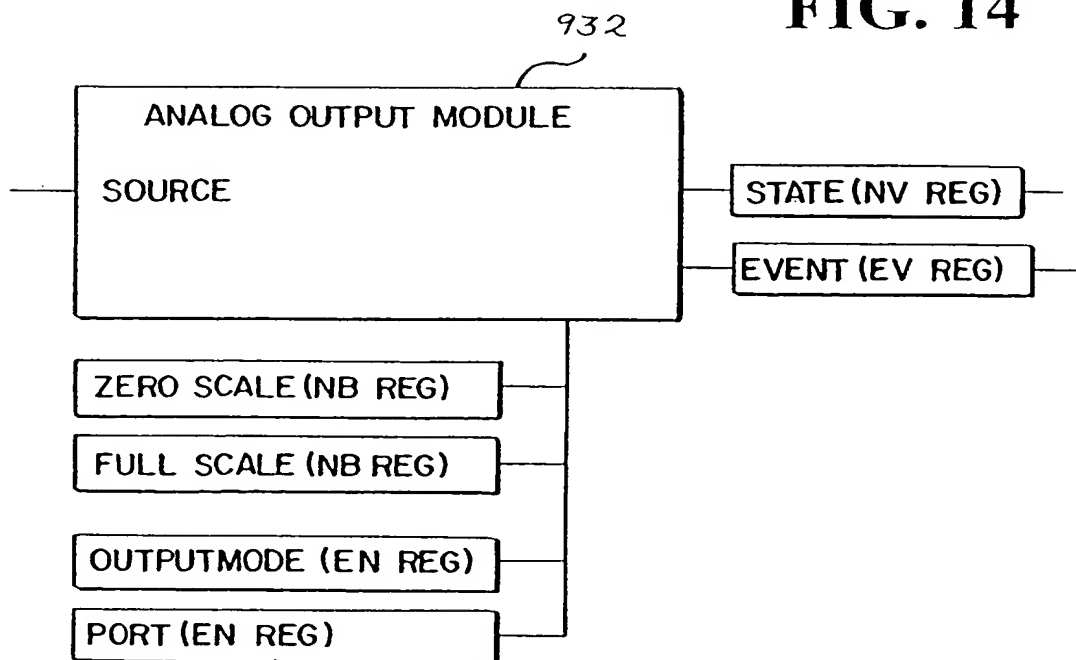


FIG. 13A

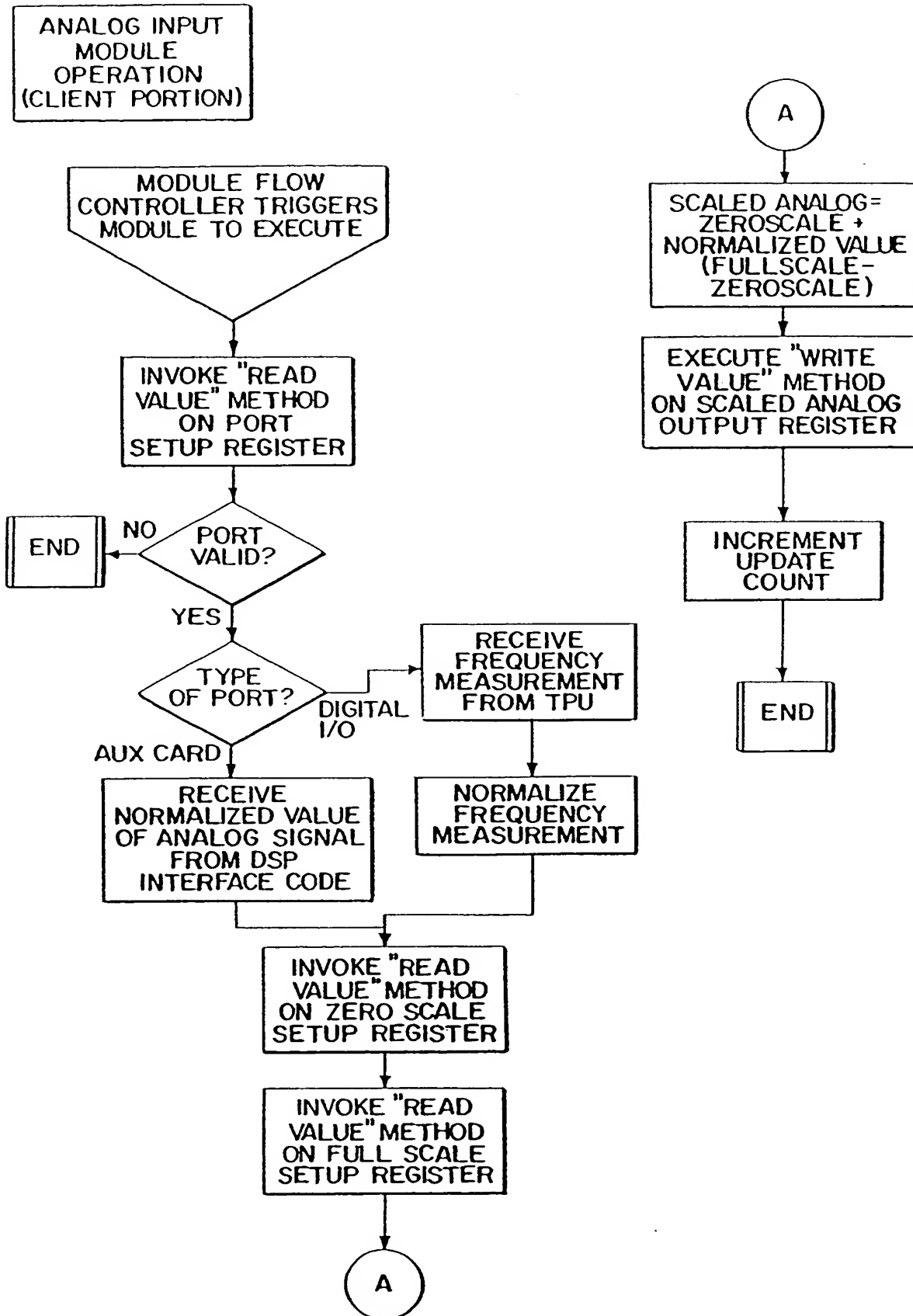


FIG. 14A

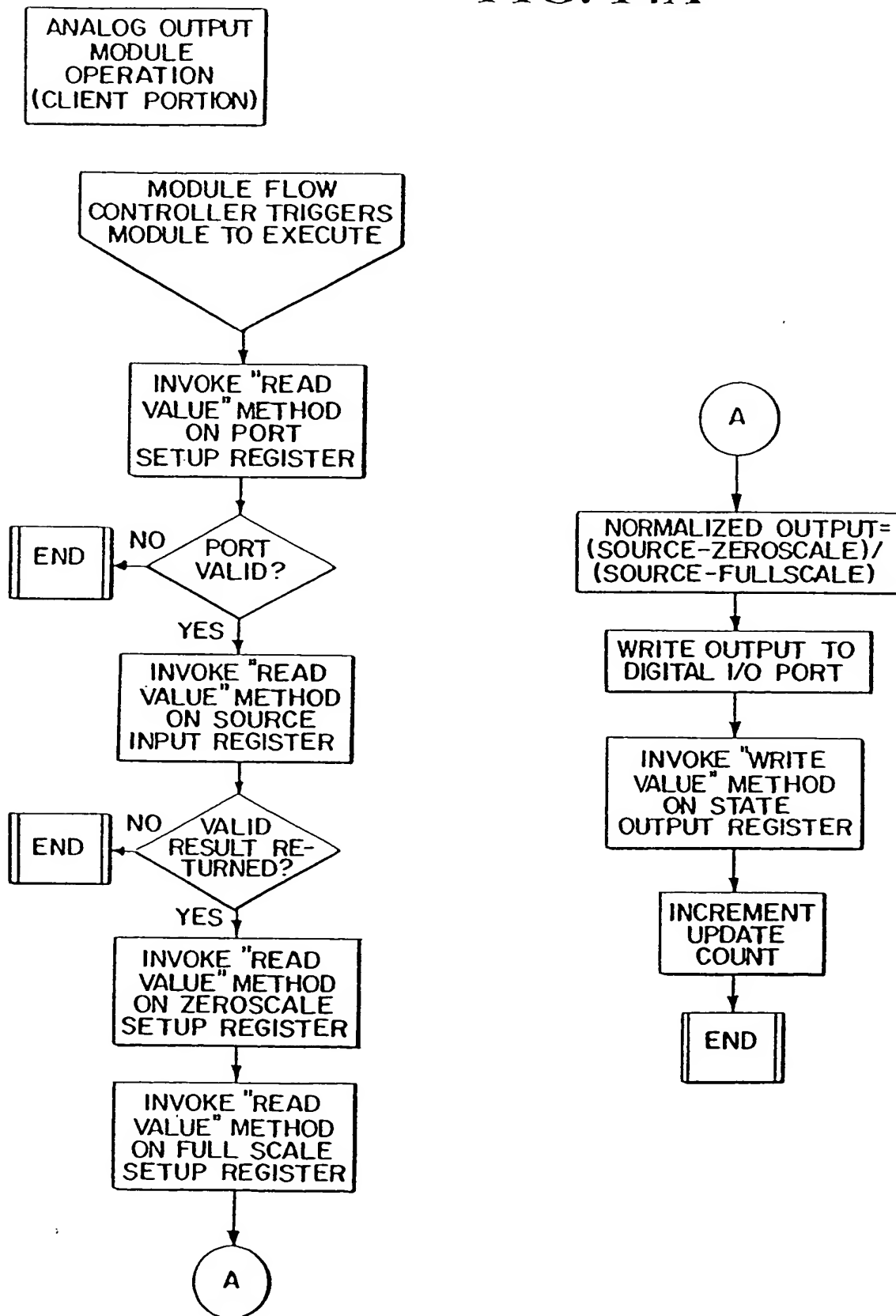


FIG. 15

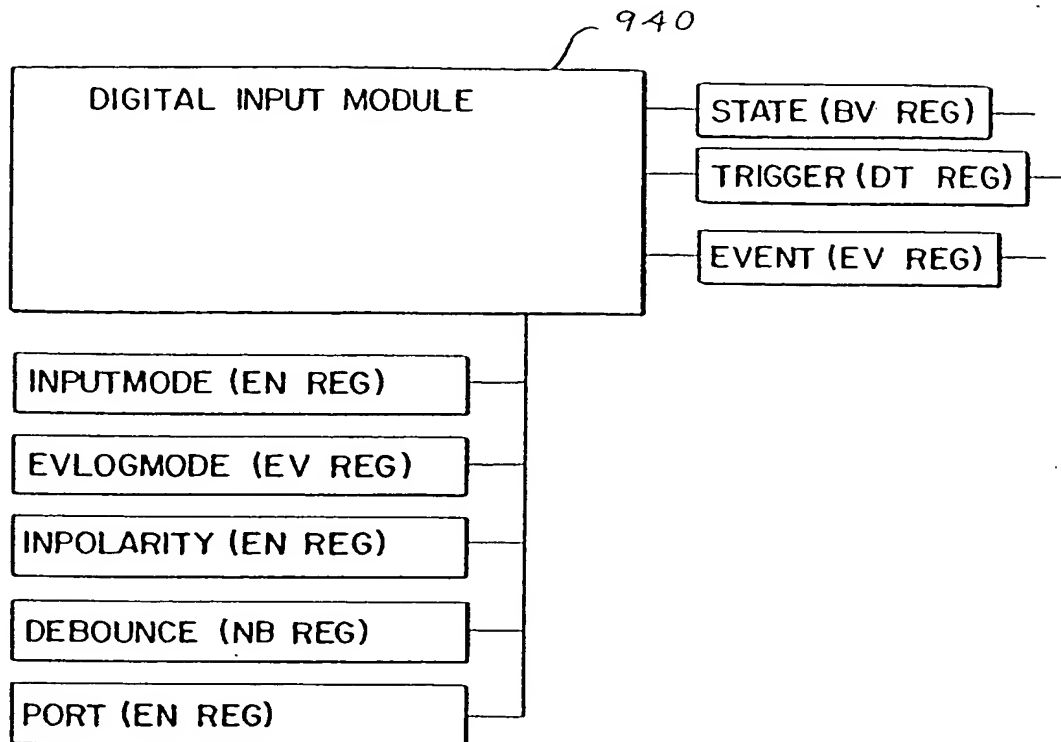


FIG. 16

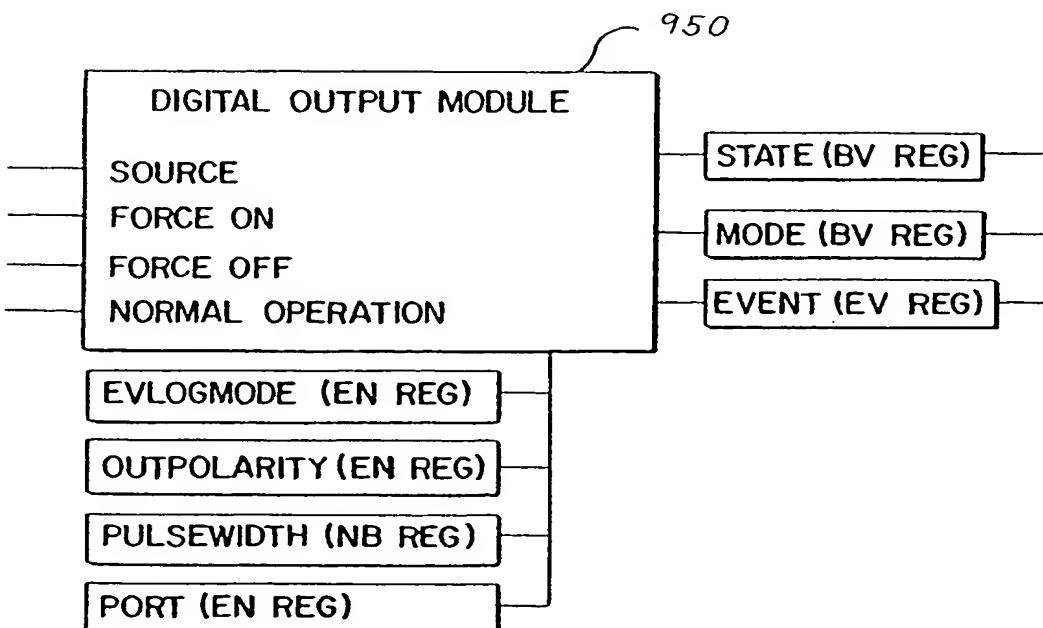


FIG. 15A

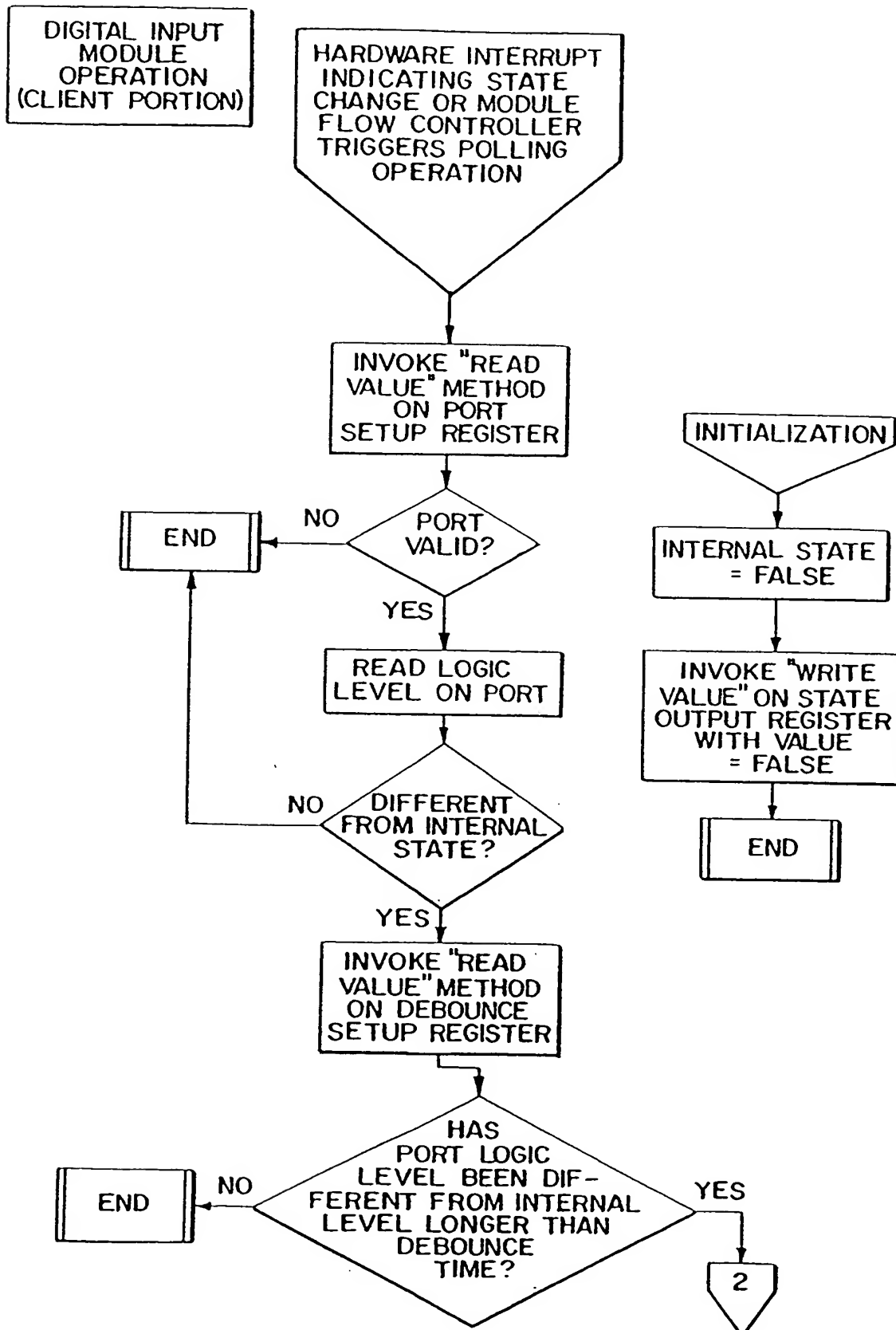
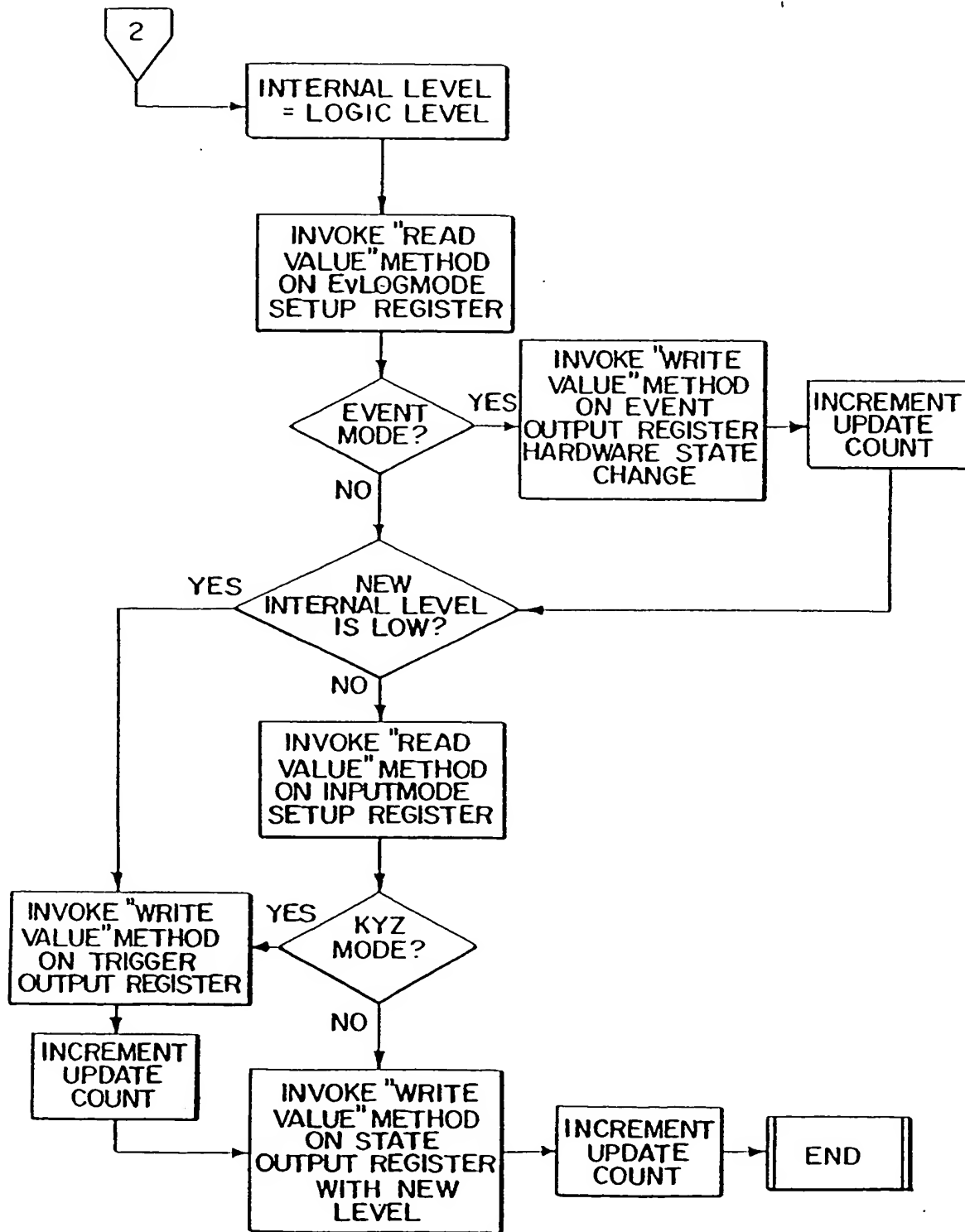


FIG. 15B





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FIG. 16A

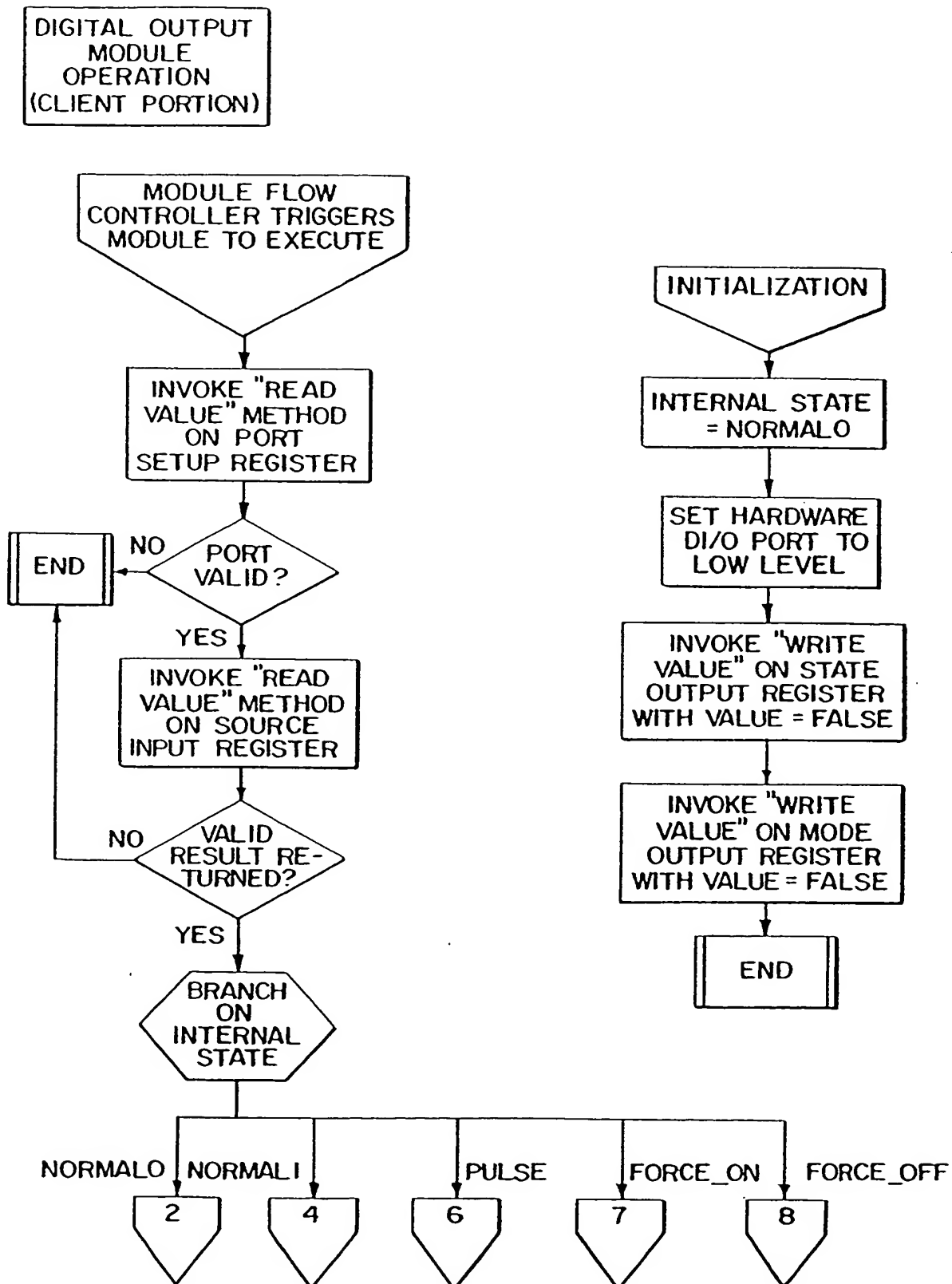


FIG. 16B

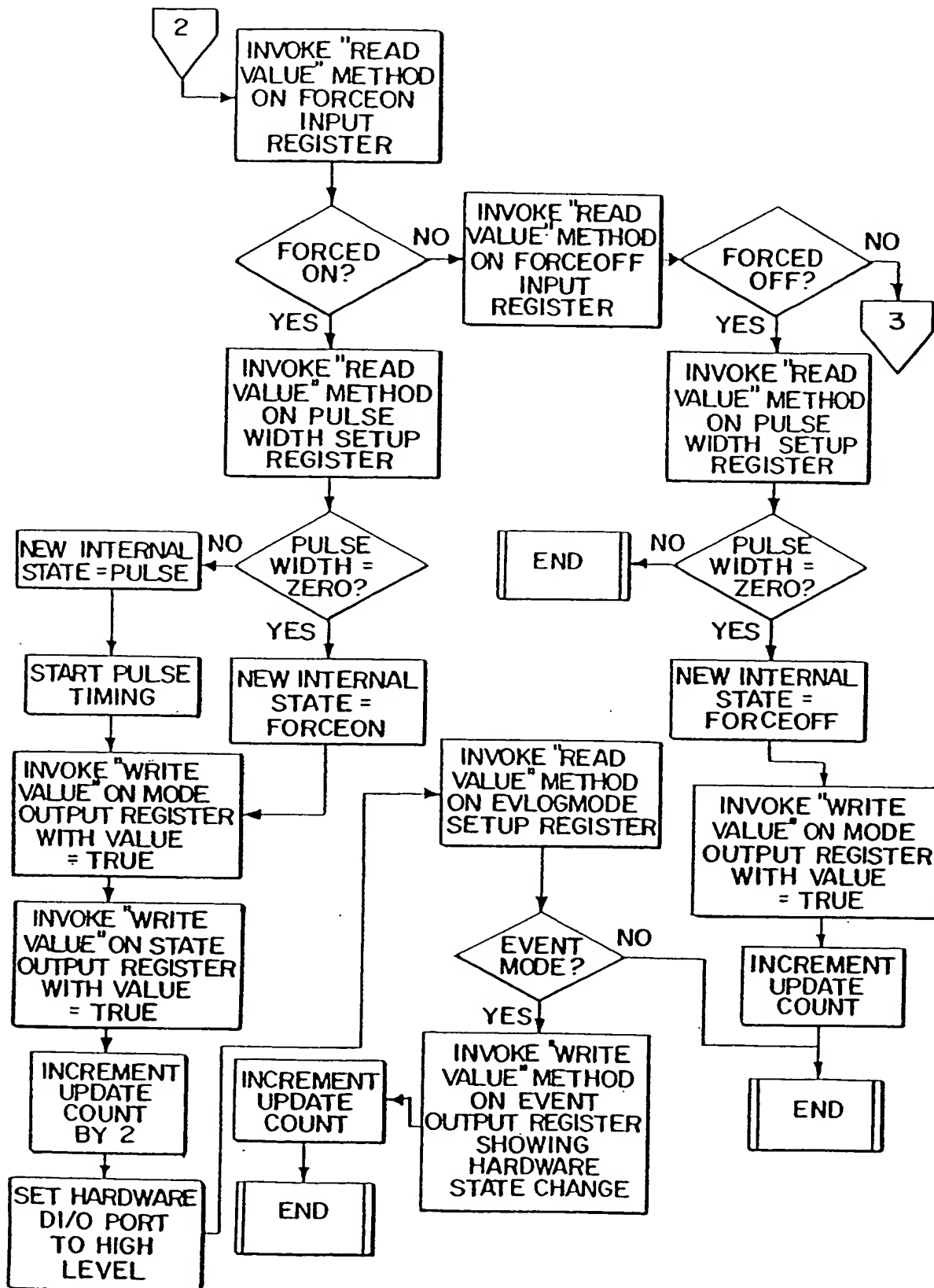


FIG. 16C

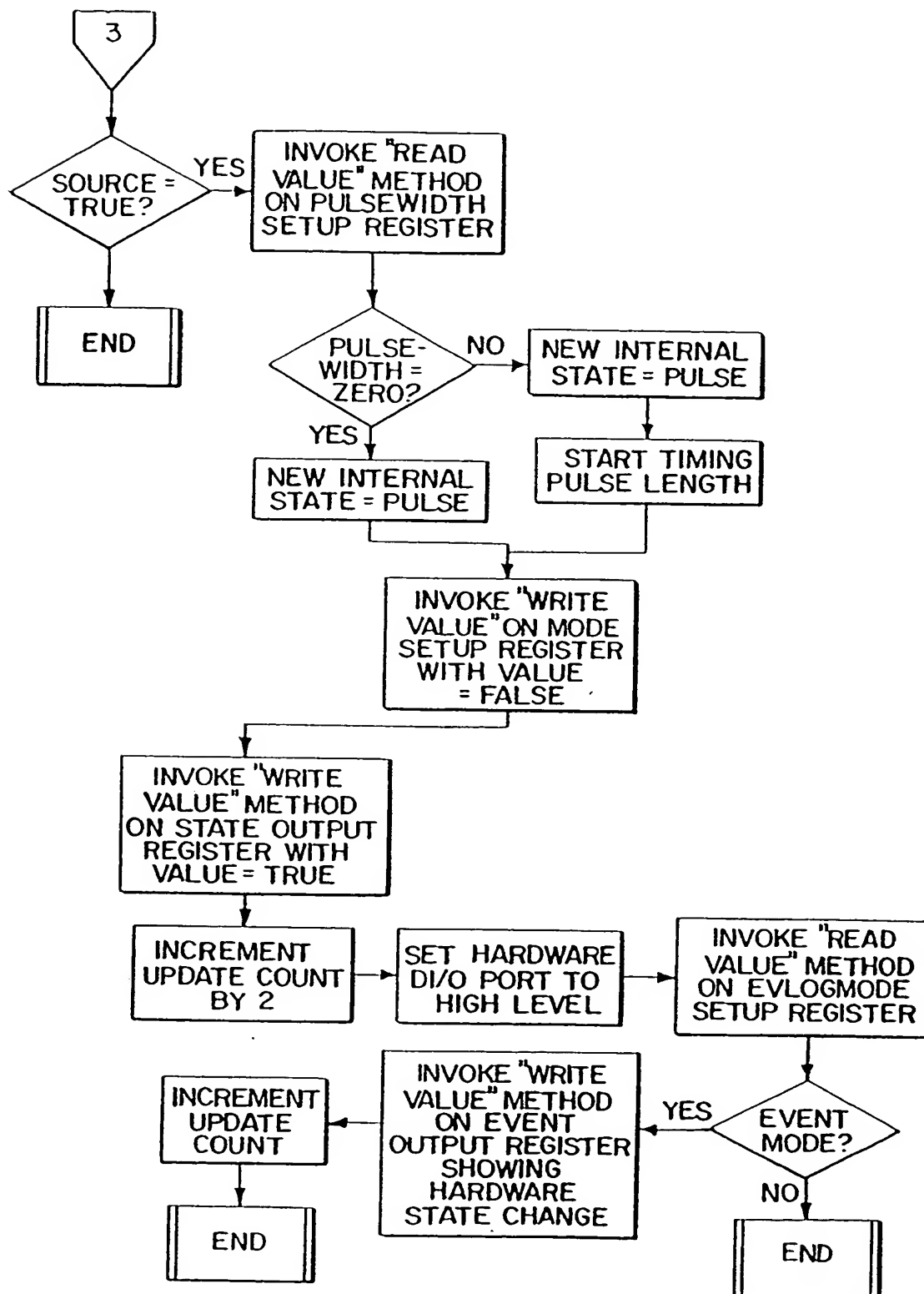


FIG. 16D

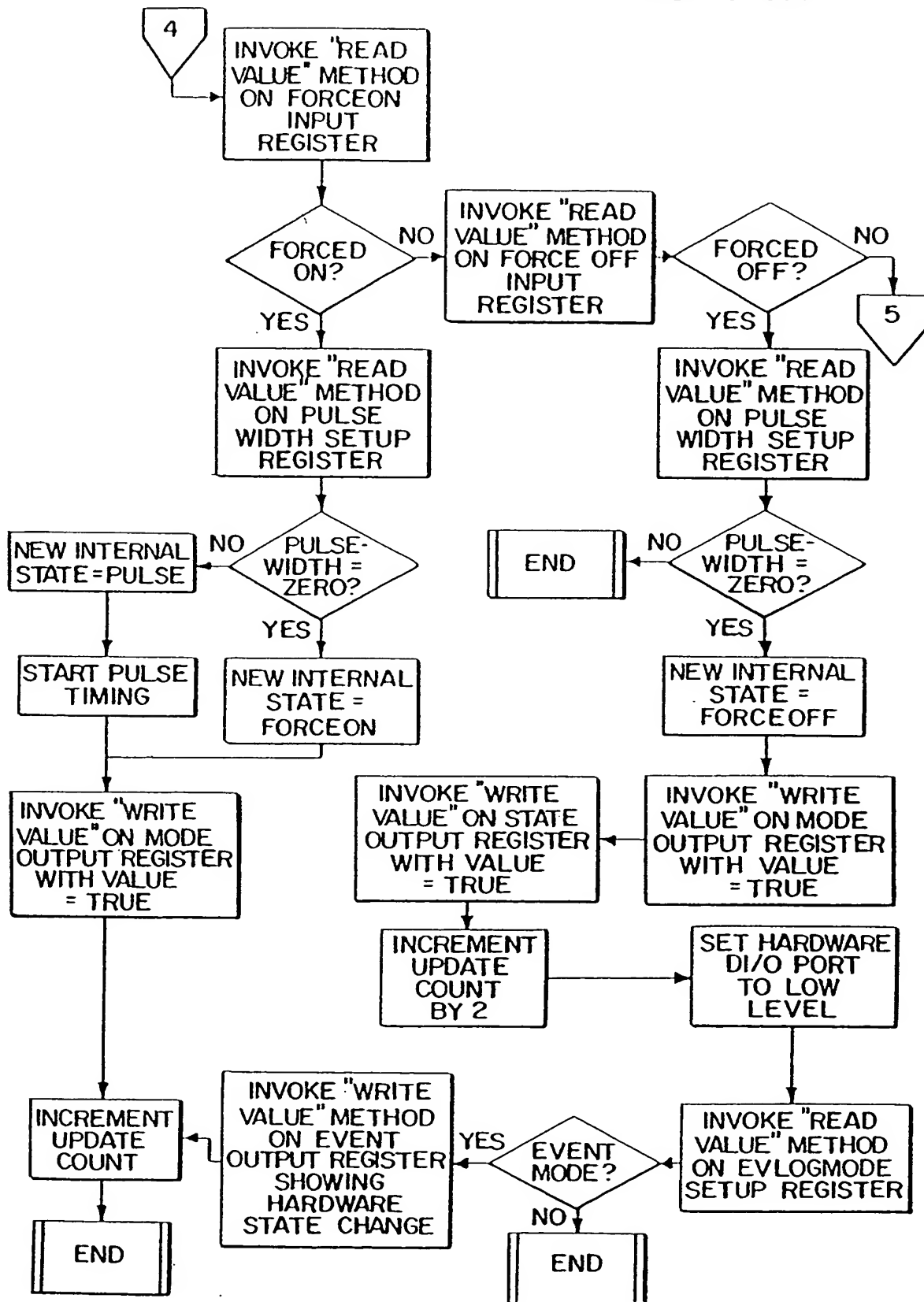


FIG. 16E

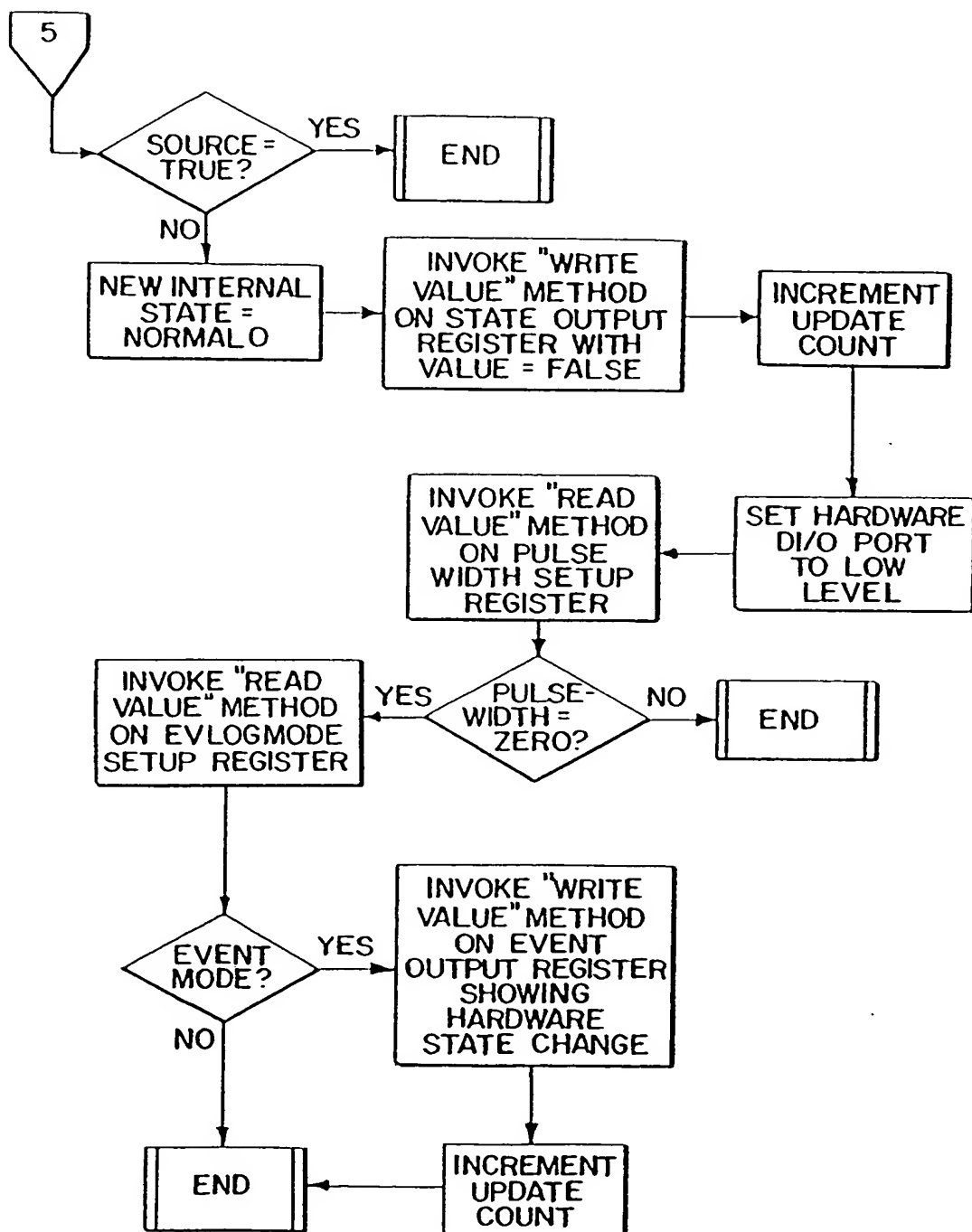


FIG. 16F

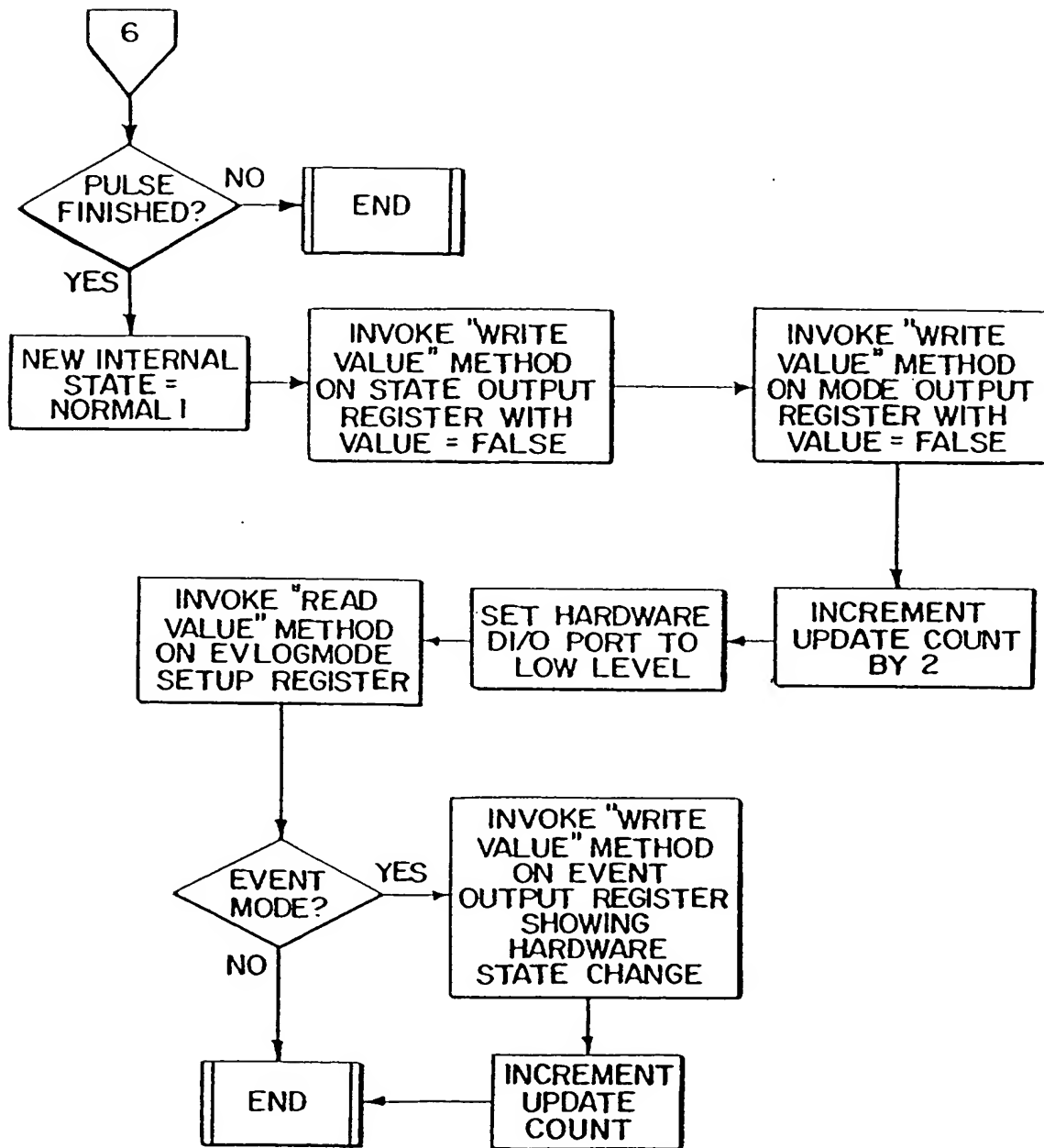


FIG. 16G

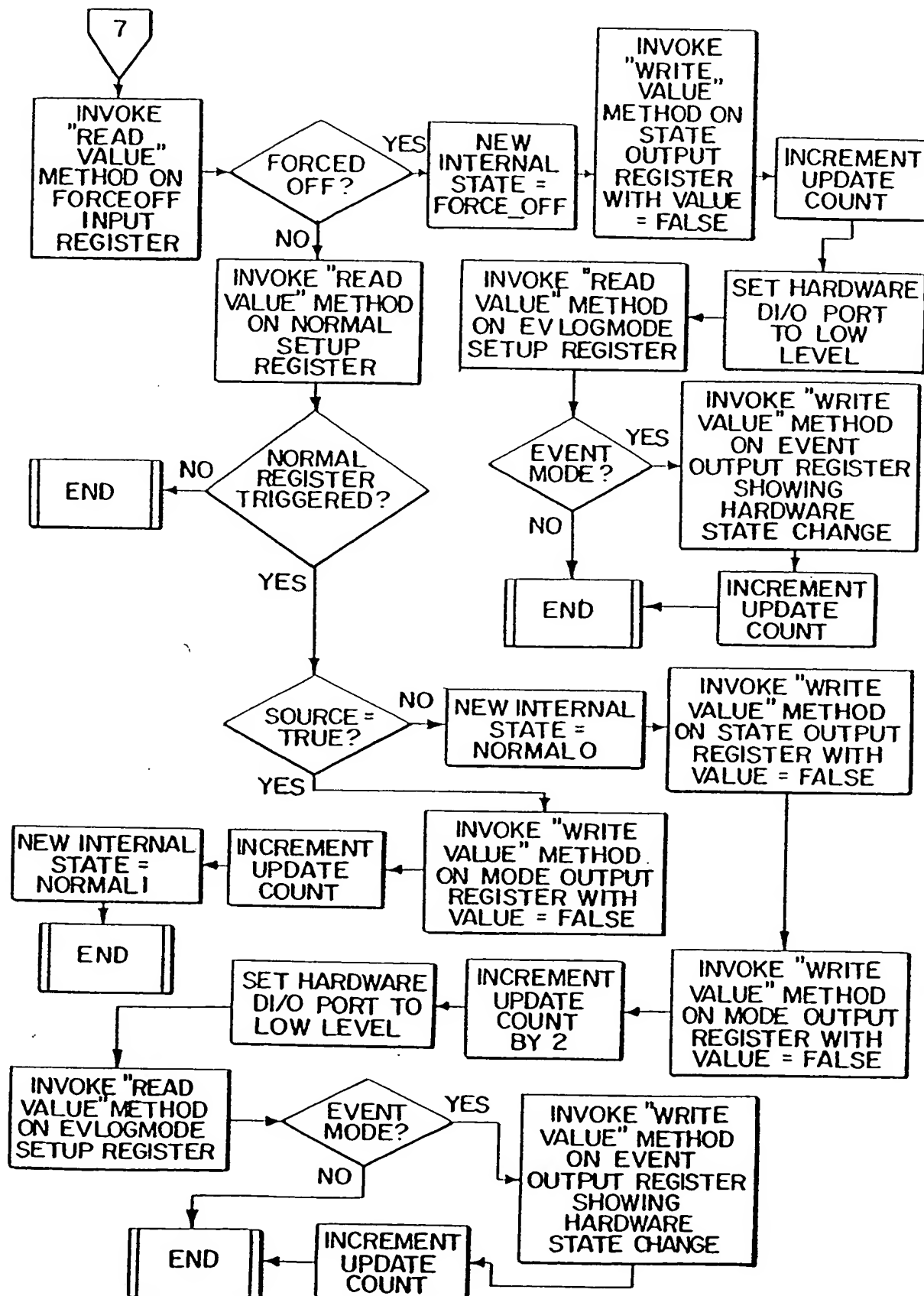


FIG. 16H

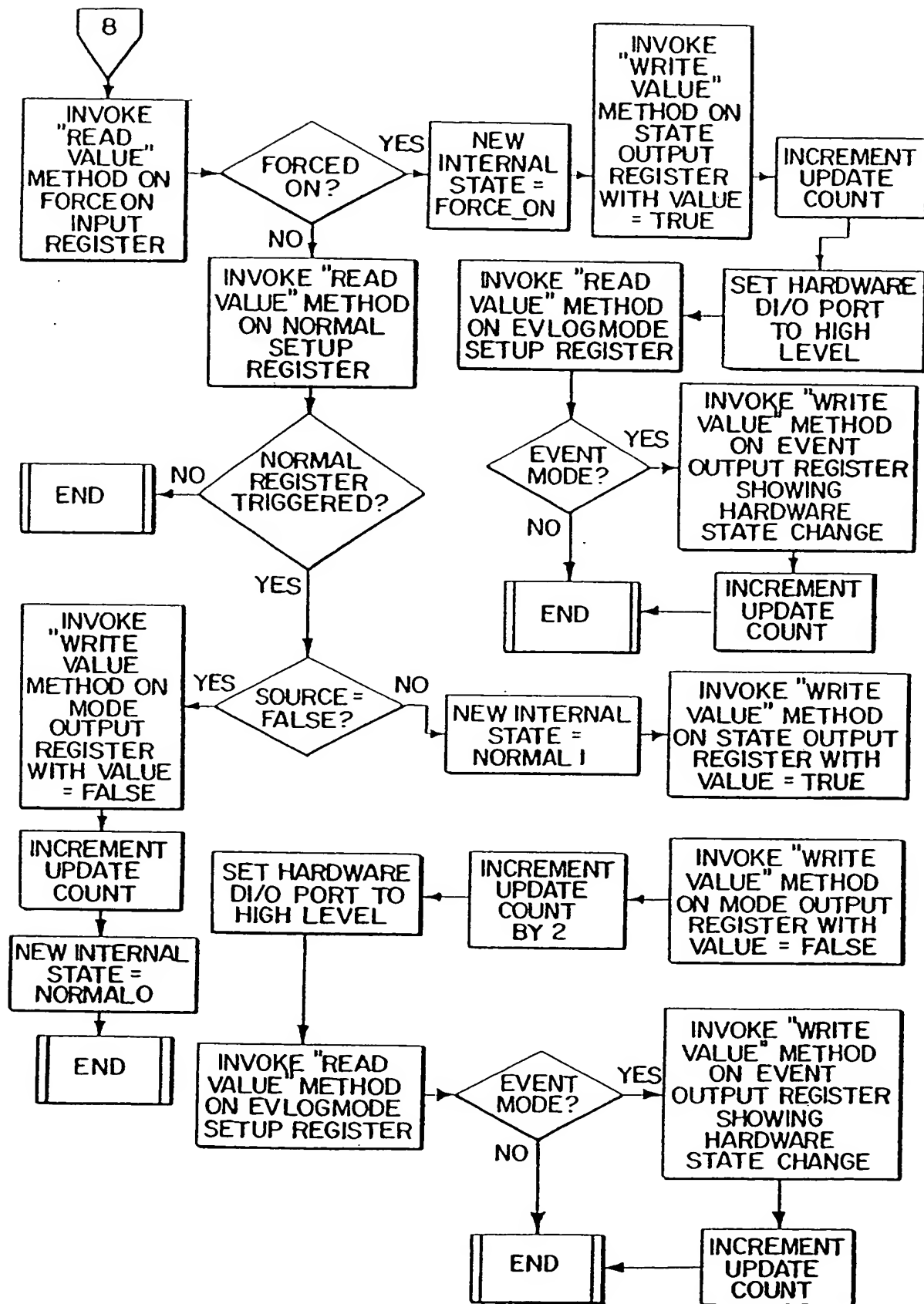




FIG. 17

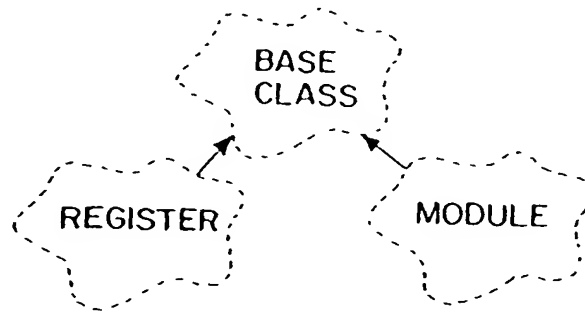
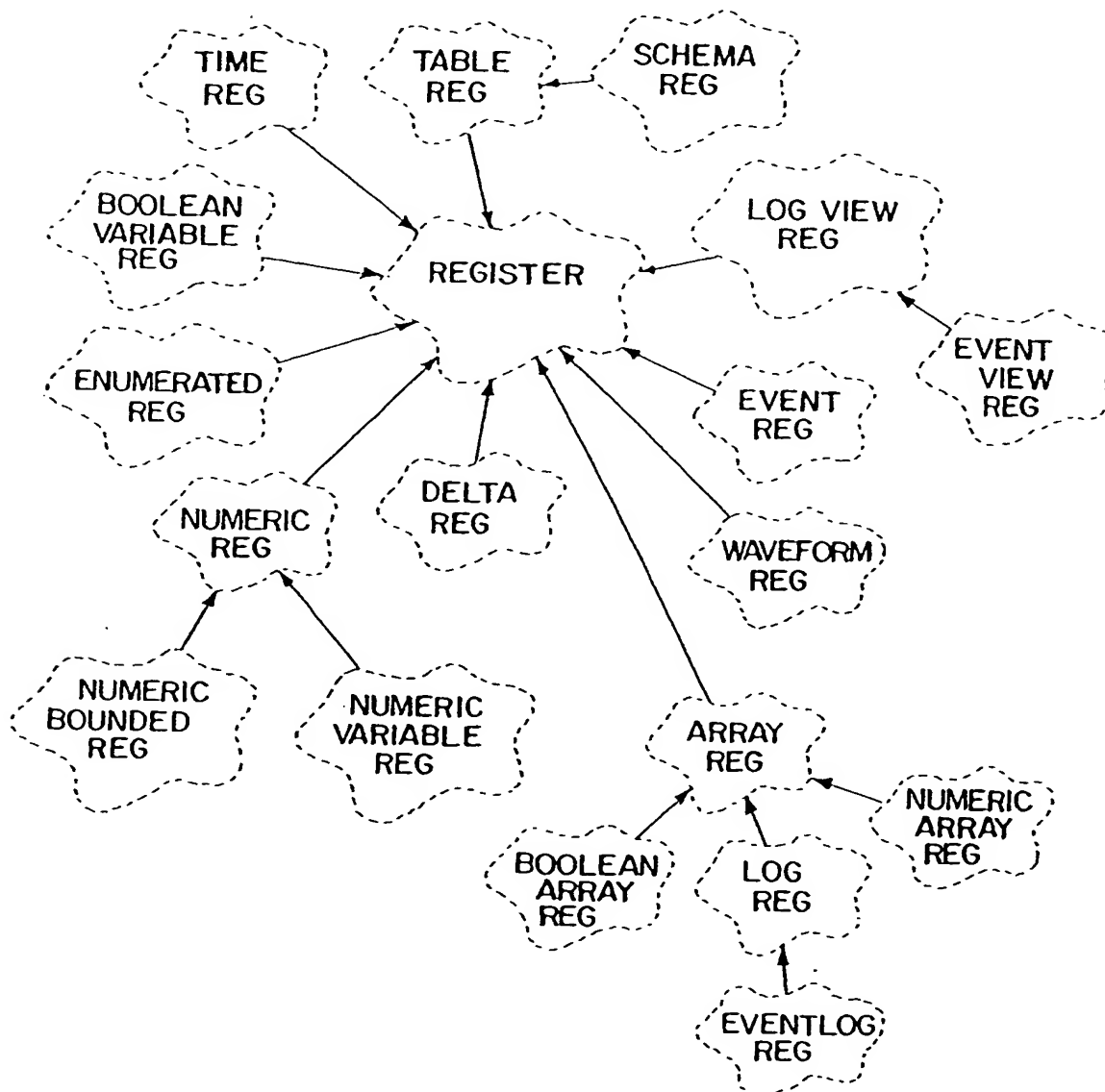


FIG. 17A



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FIG. 17B

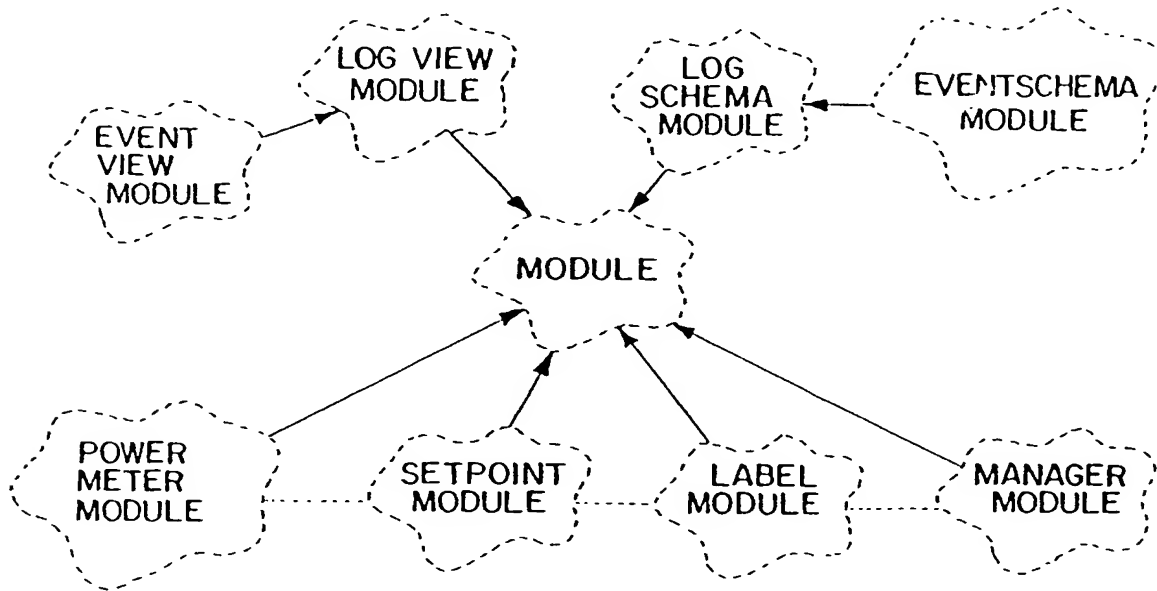


FIG. 17C

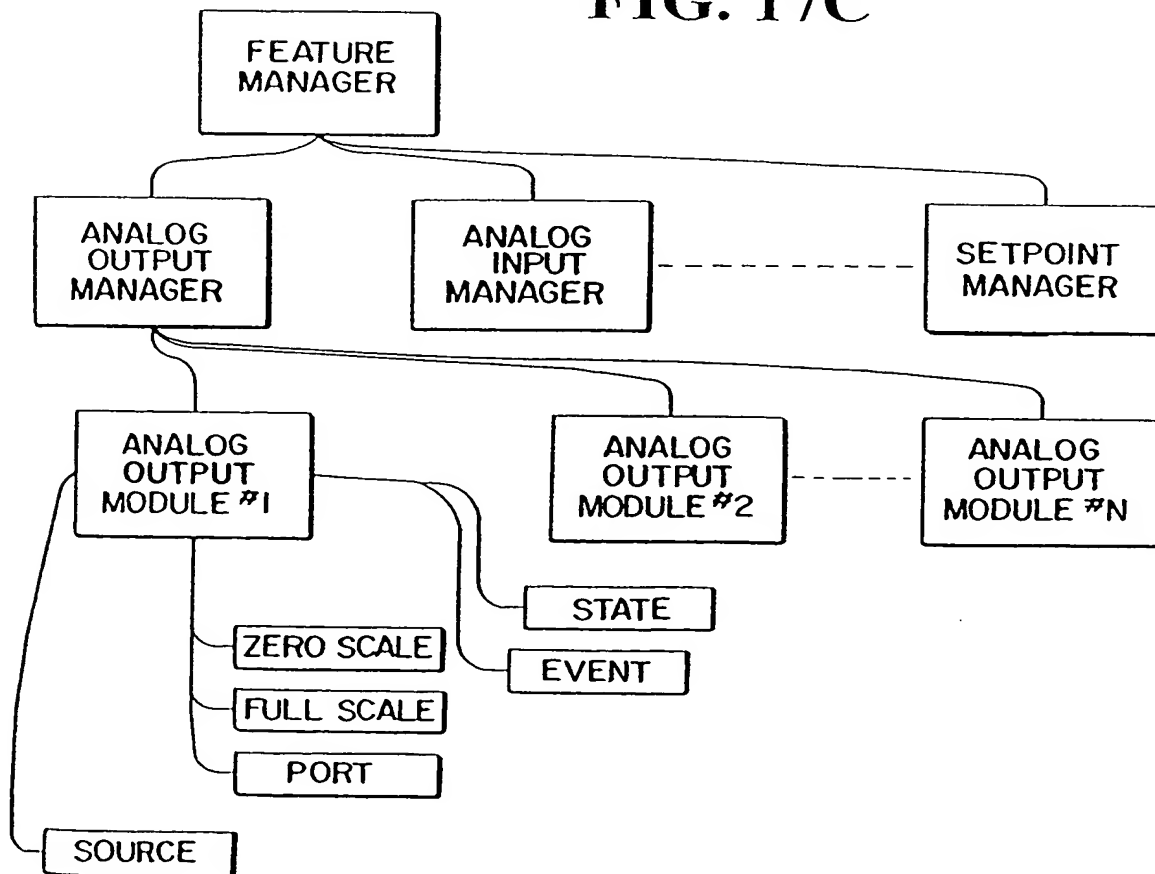


FIG. 18

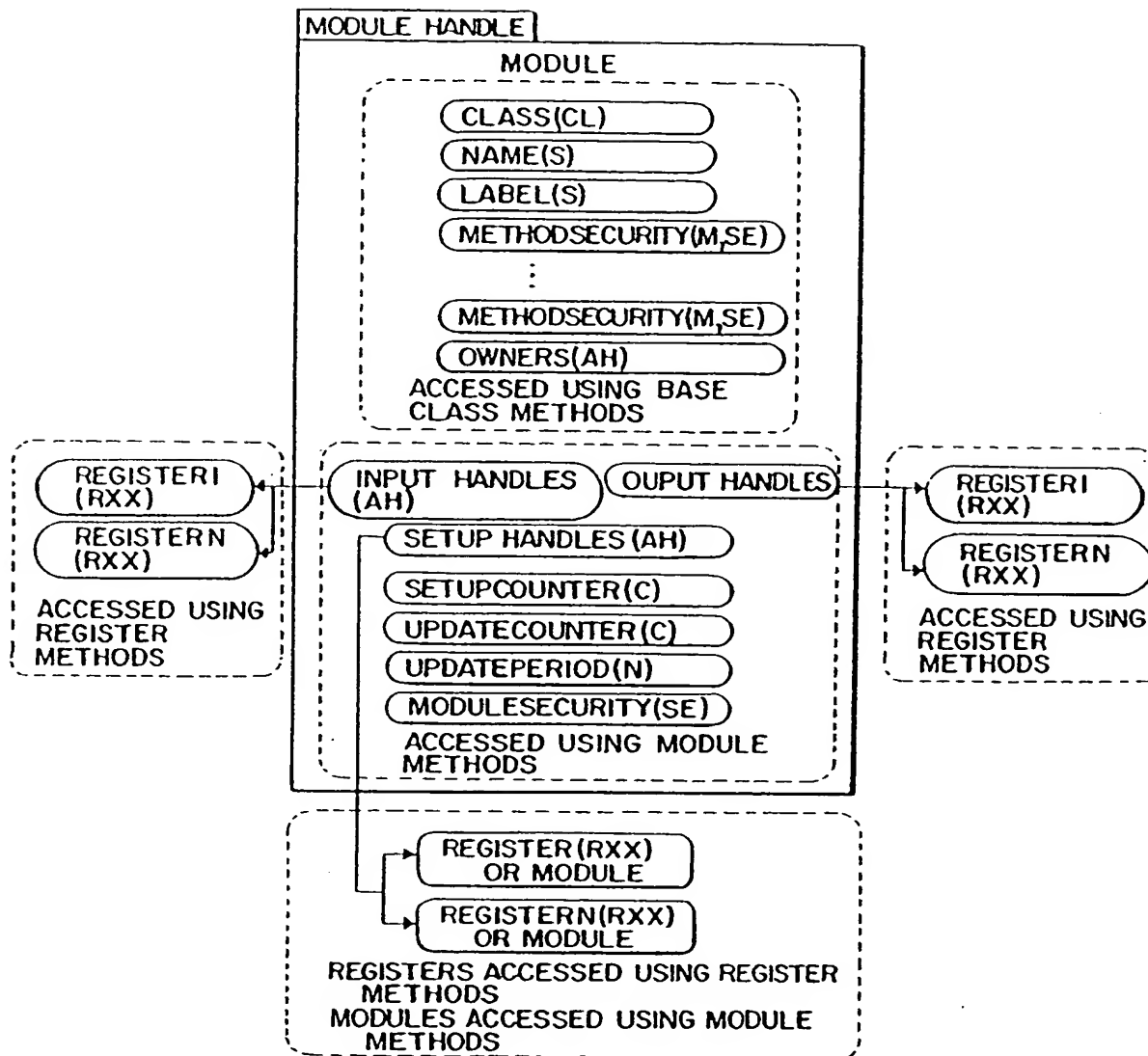
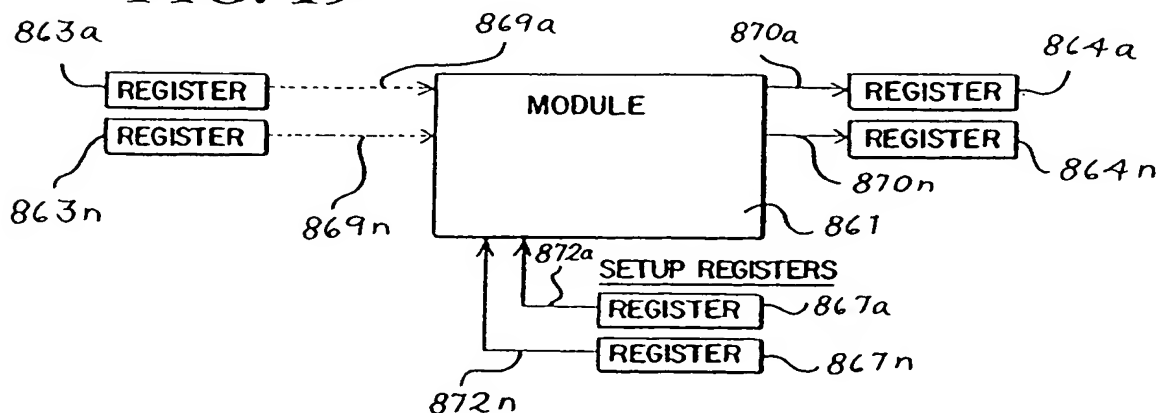


FIG. 19



40 07 07

FIG. 19A

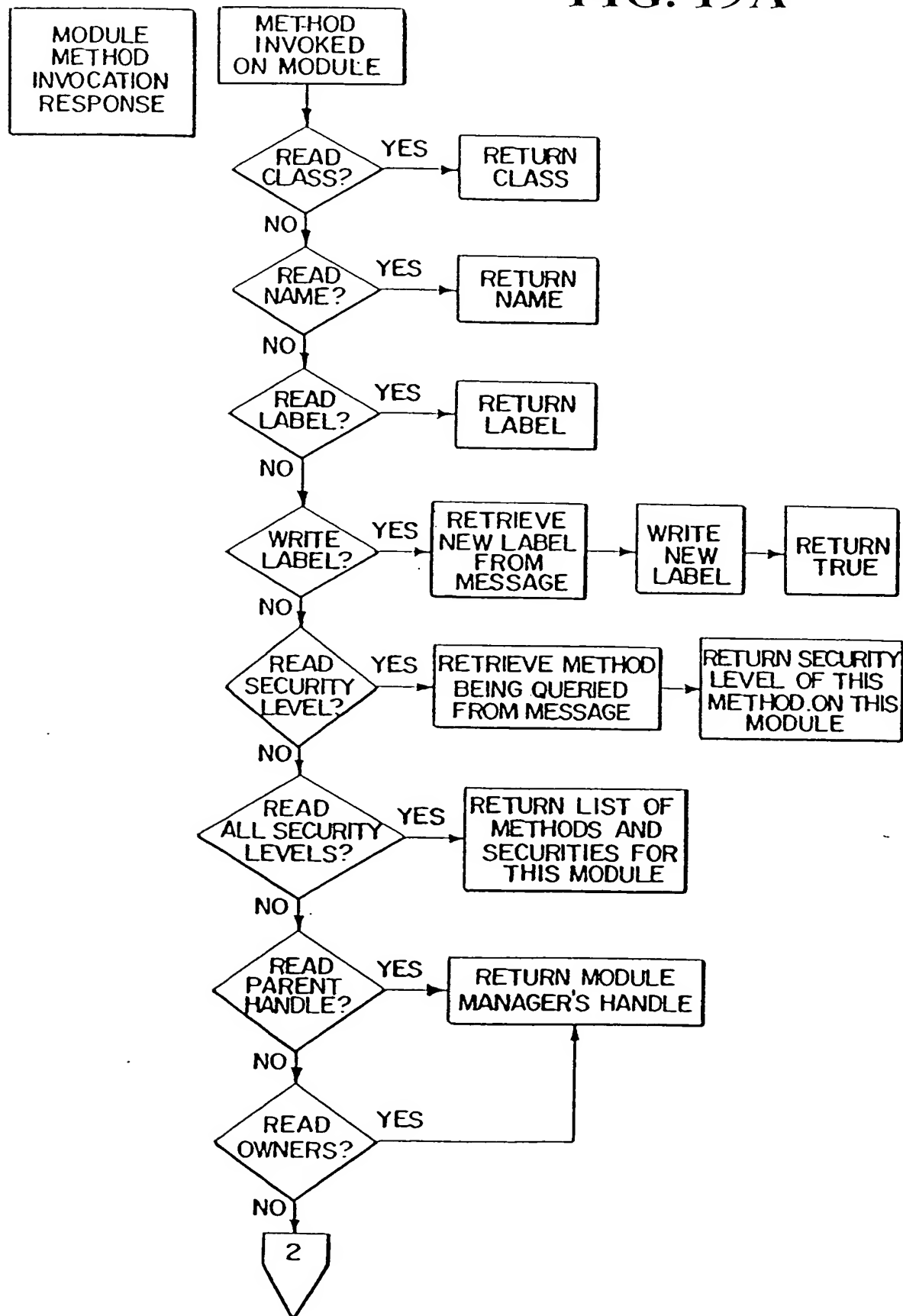


FIG. 19B

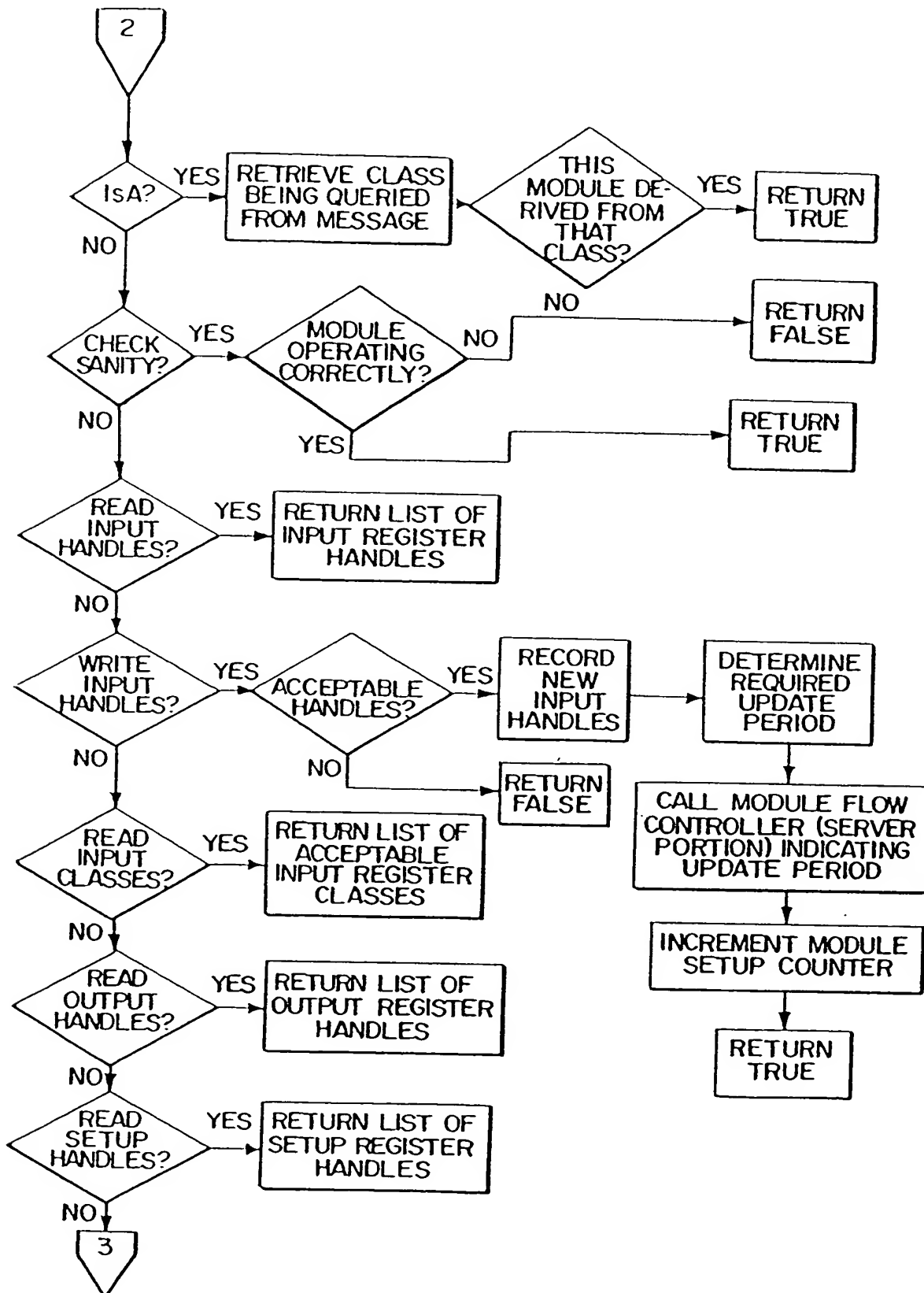


FIG. 19C

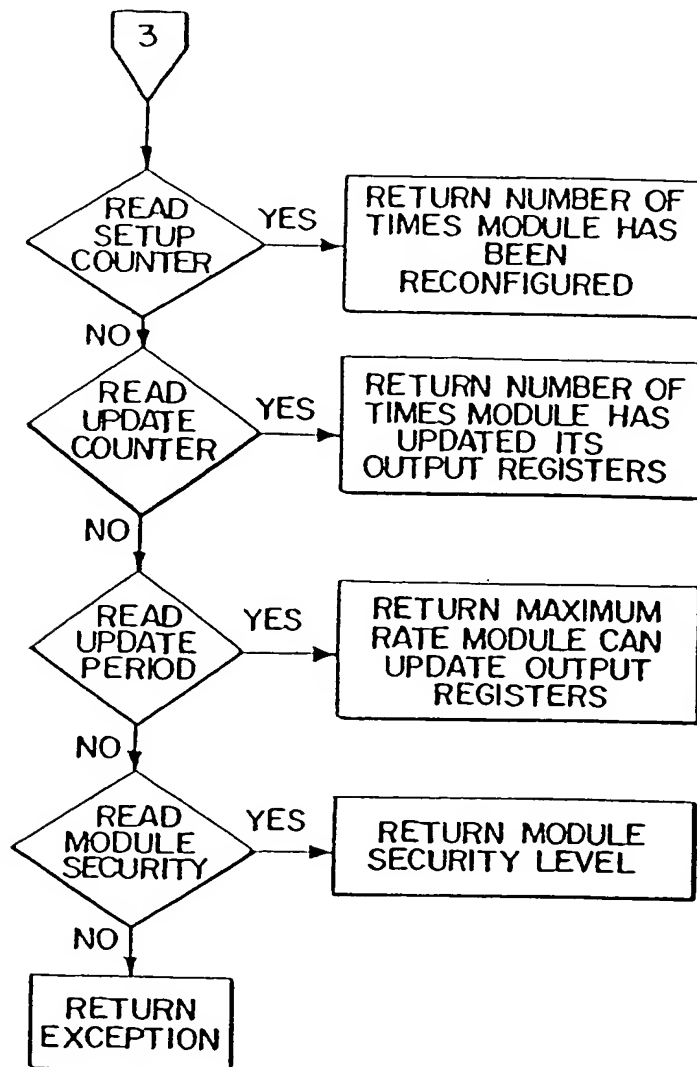


FIG. 20

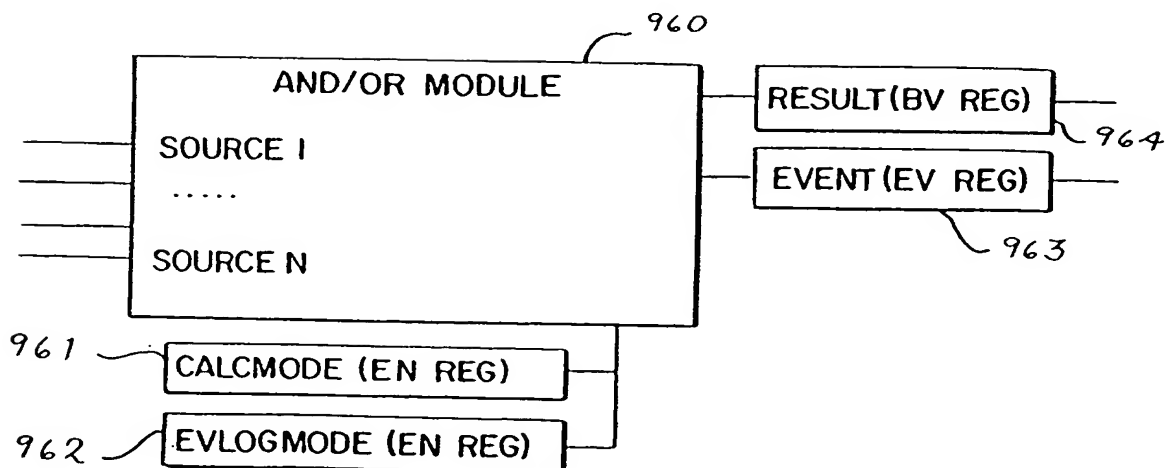


FIG. 20A

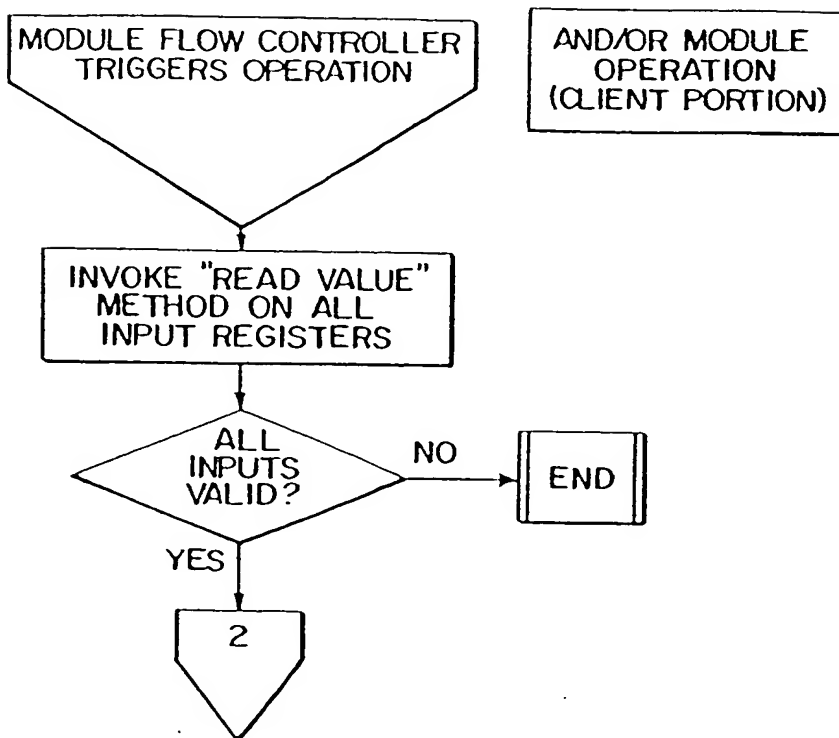


FIG. 21

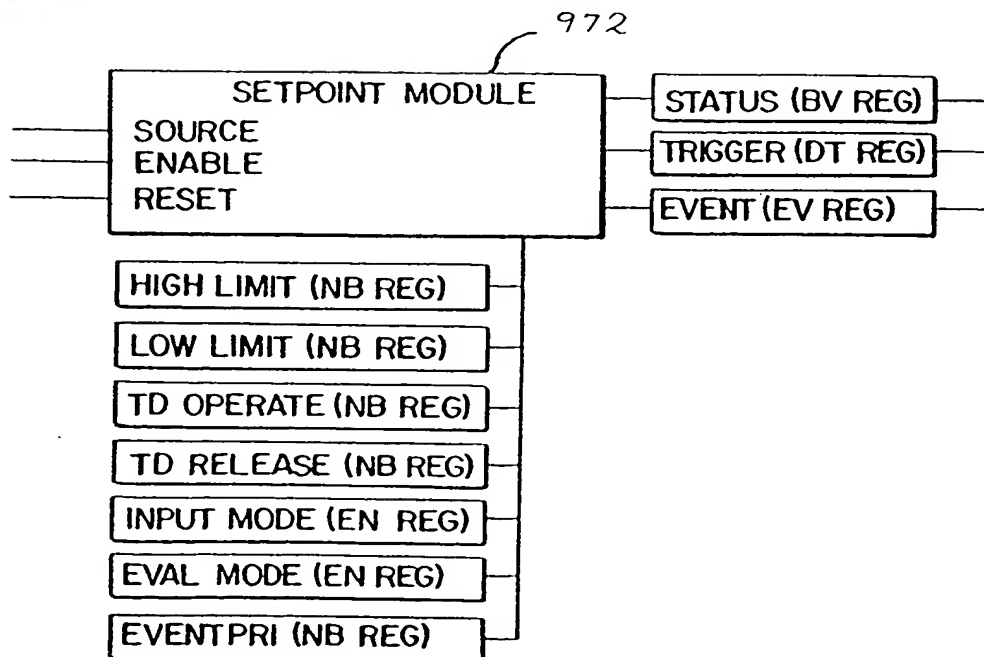


FIG. 20B

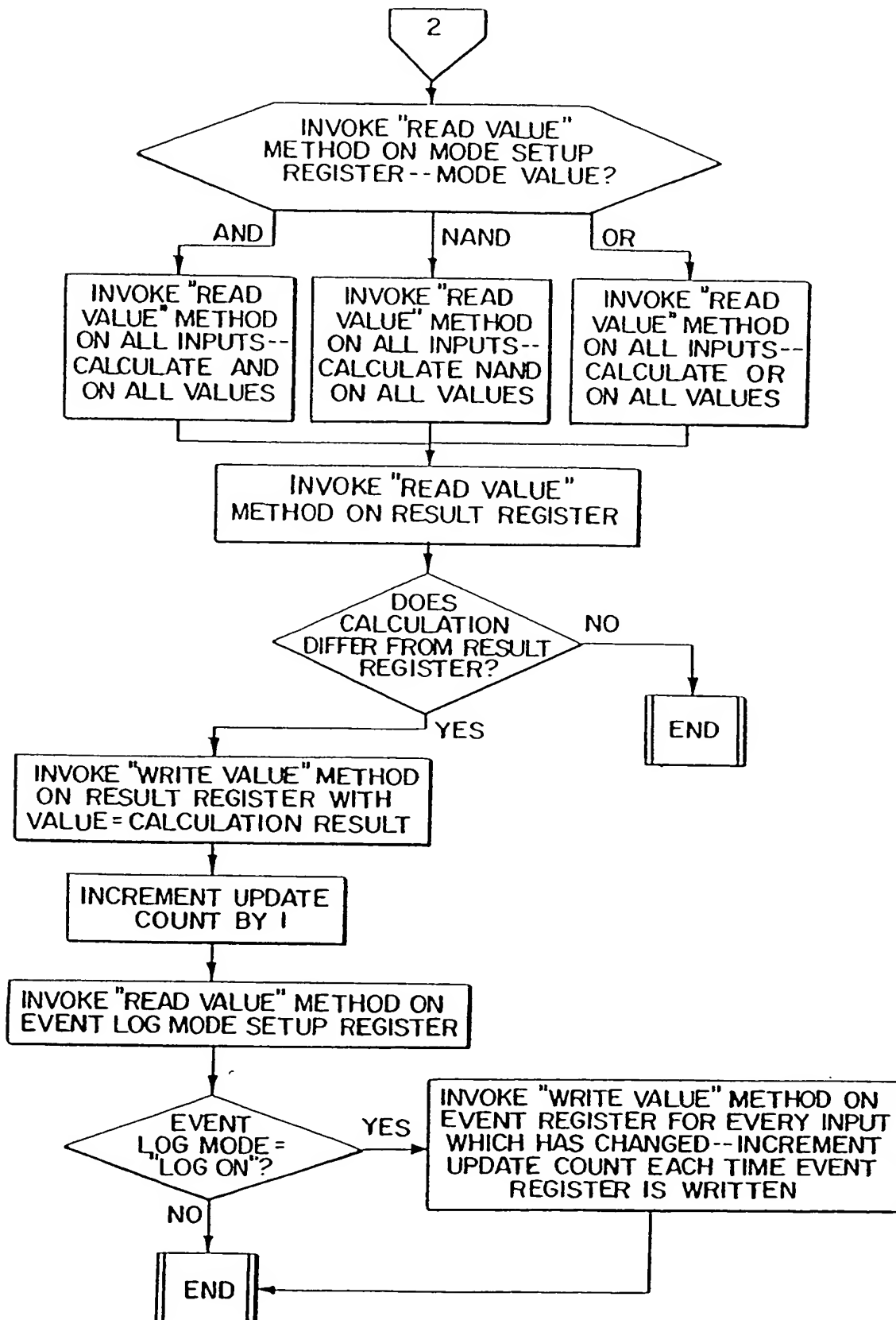




FIG. 21A

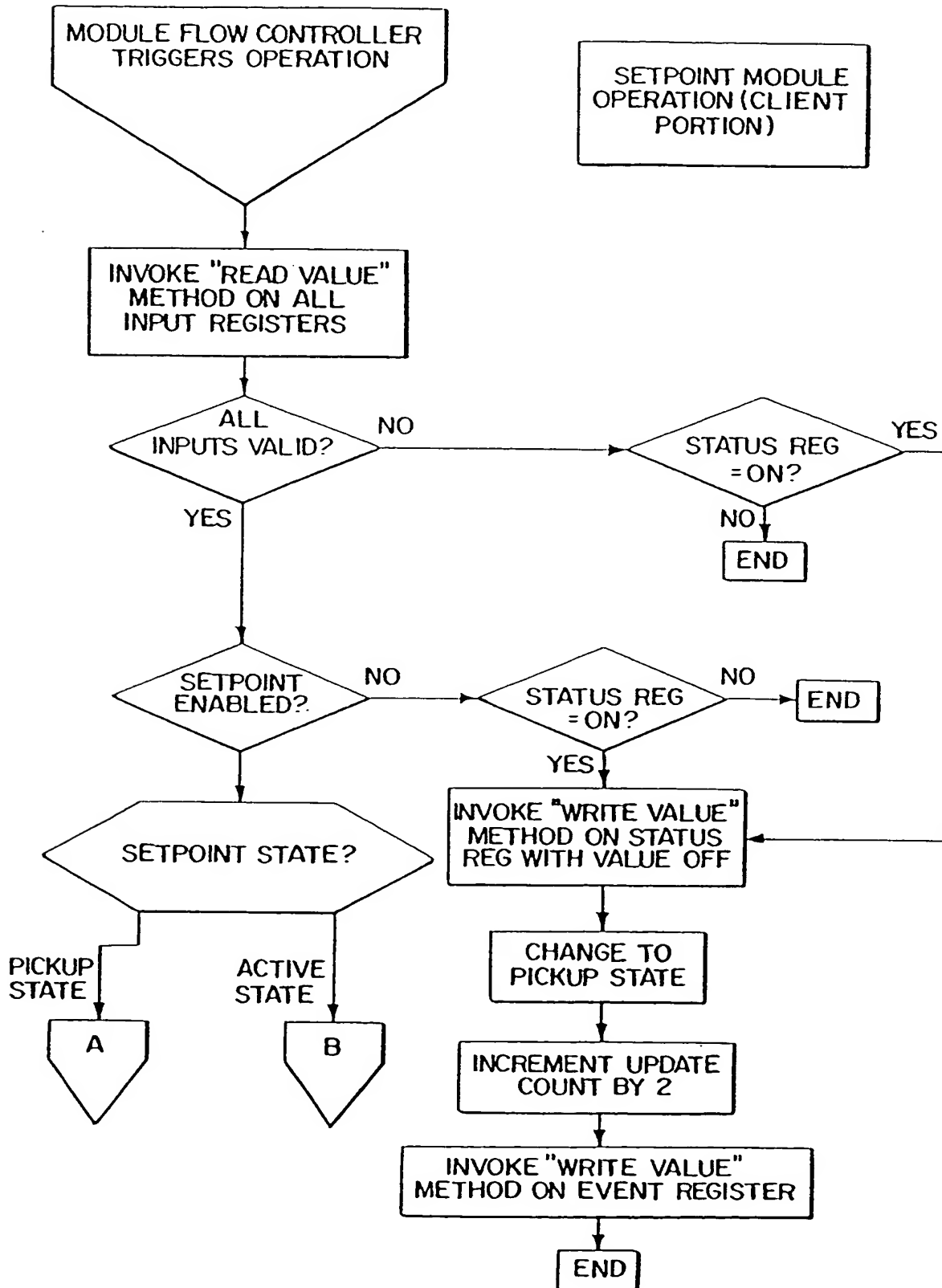


FIG. 21B

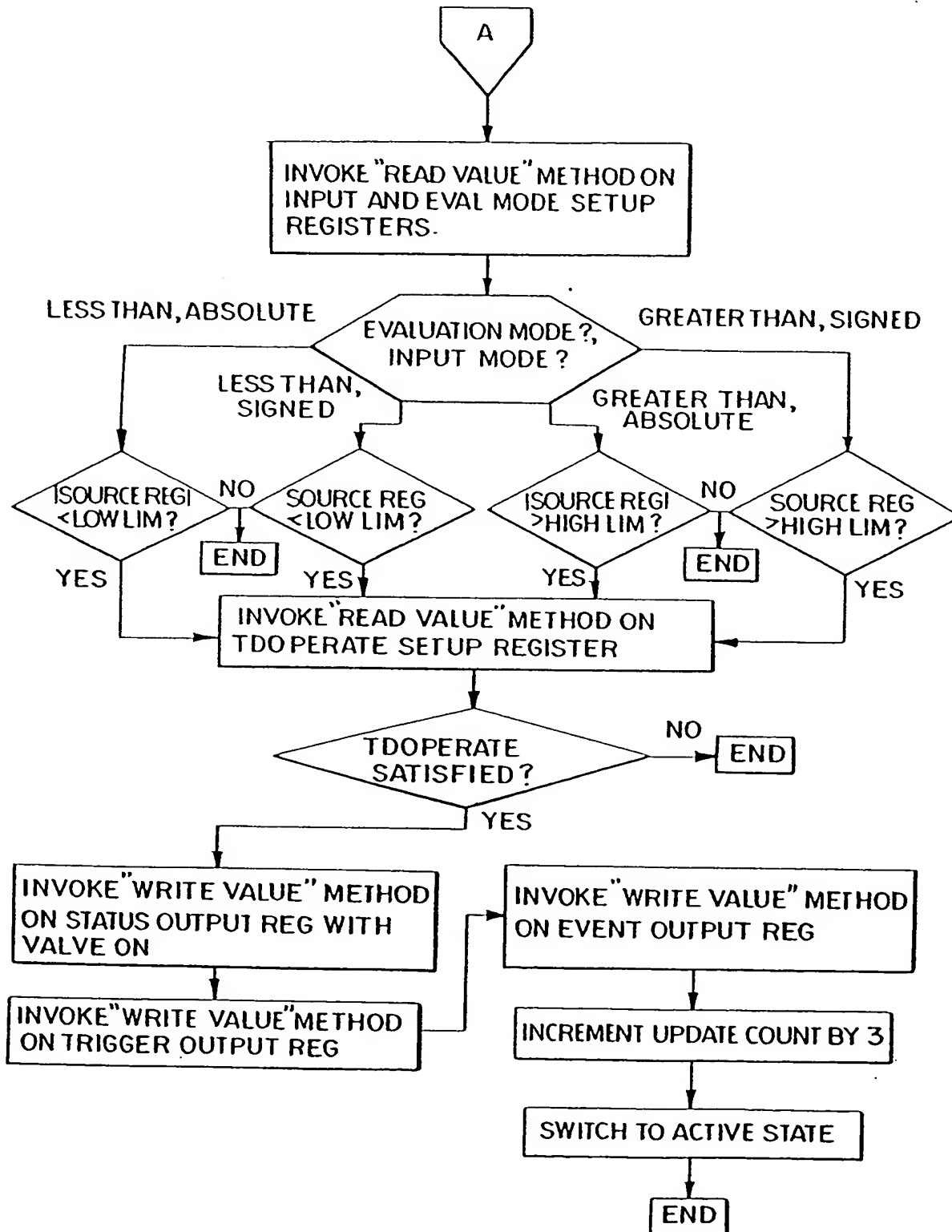


FIG. 21C

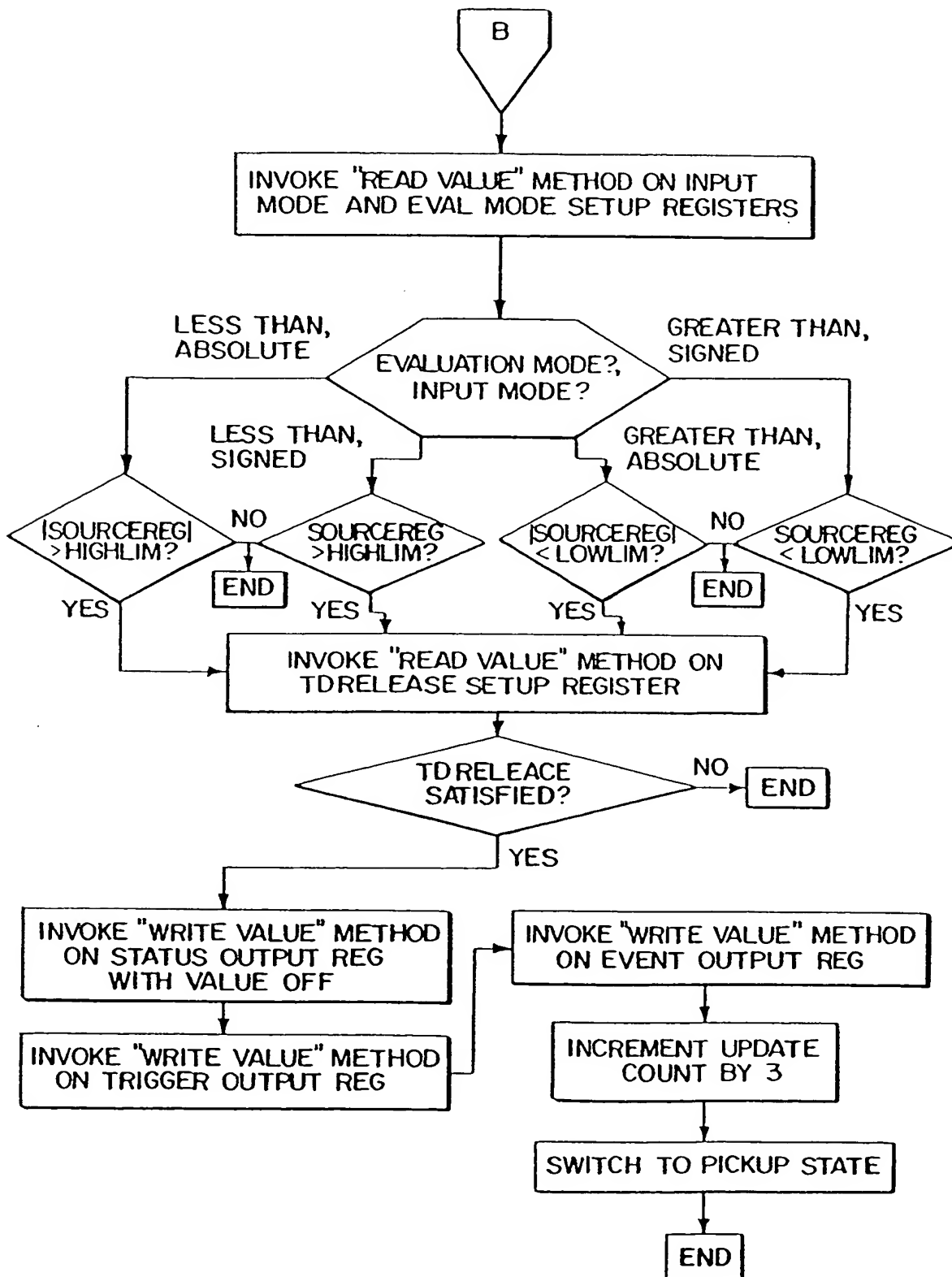


FIG. 22

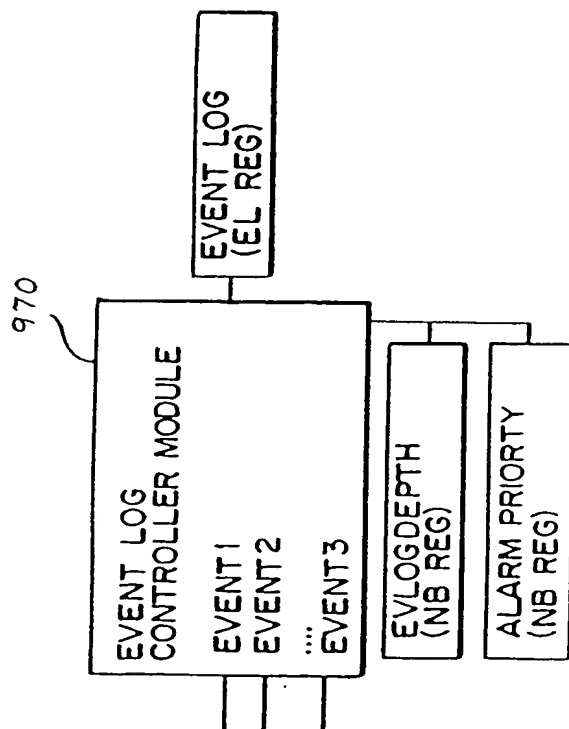


FIG. 22A

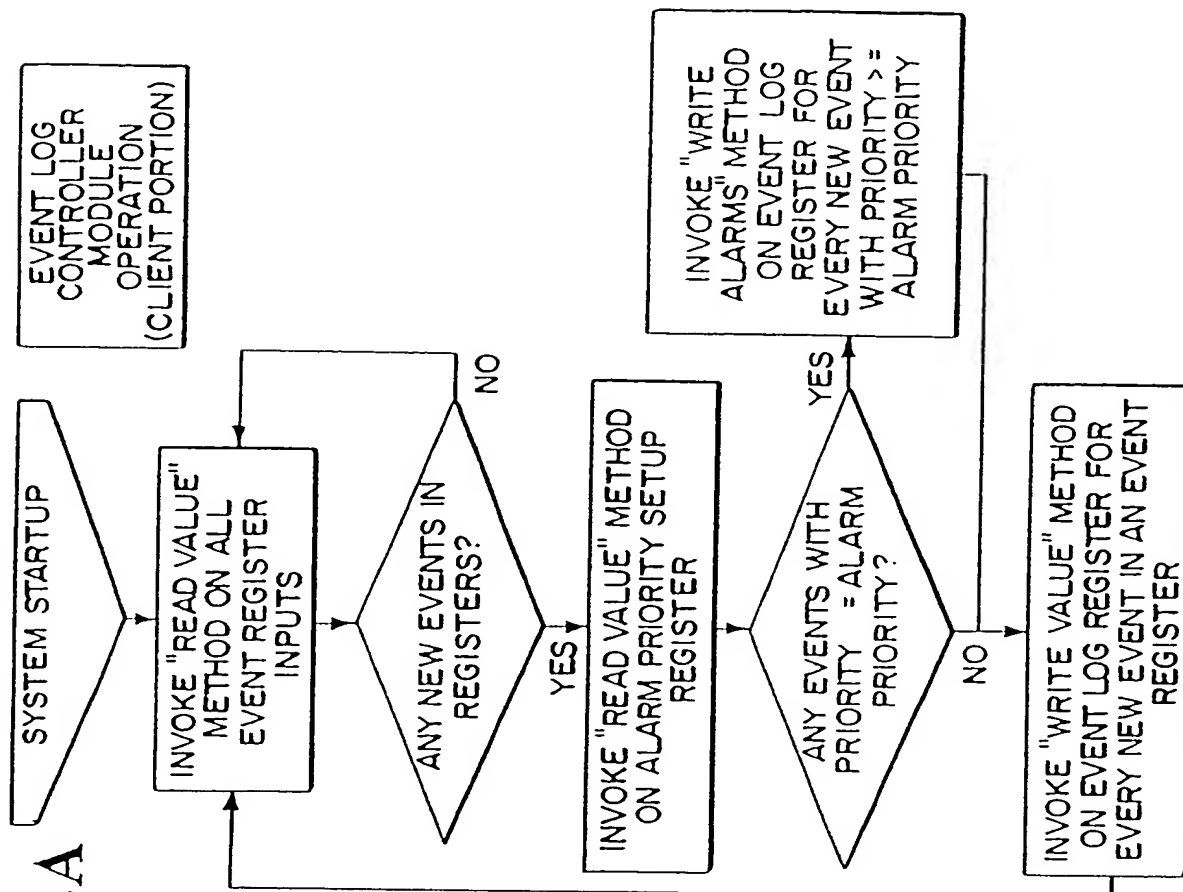


FIG. 23

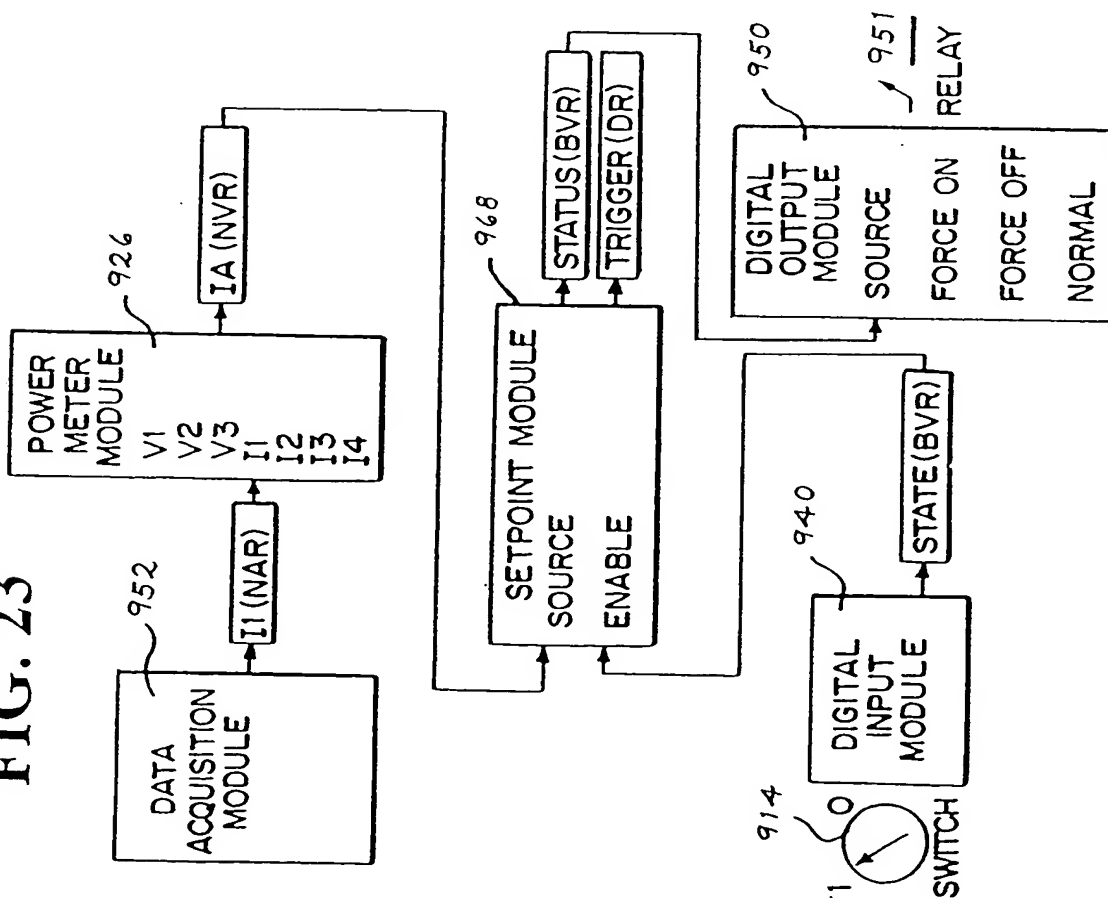
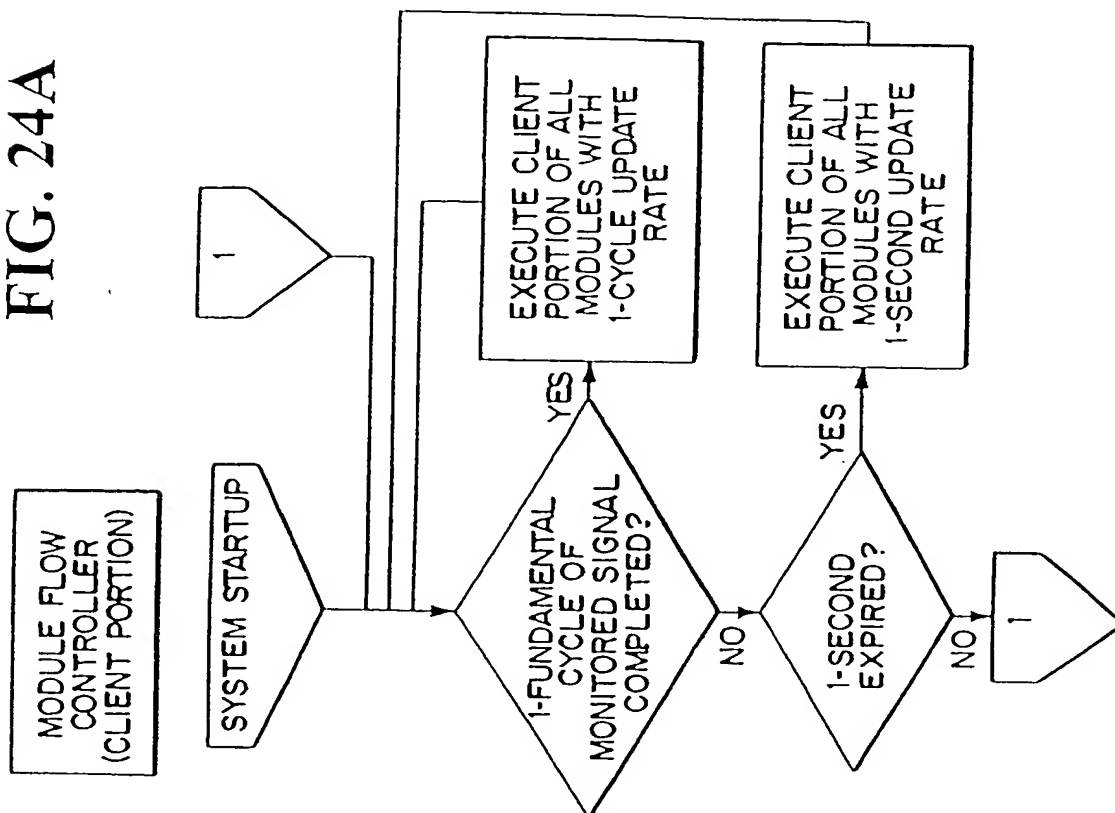


FIG. 24A



50 86 007

FIG. 25

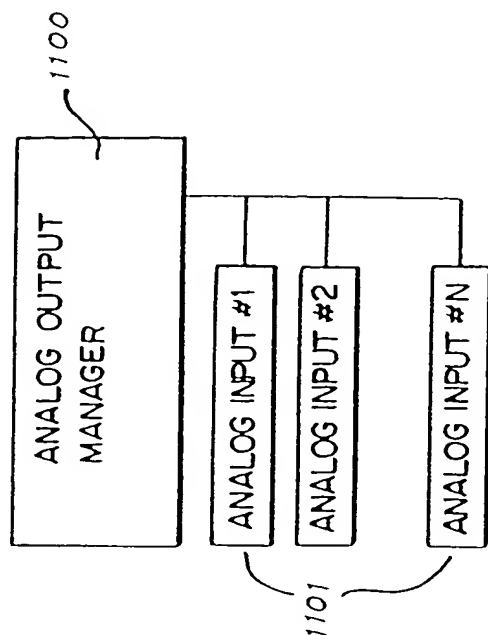
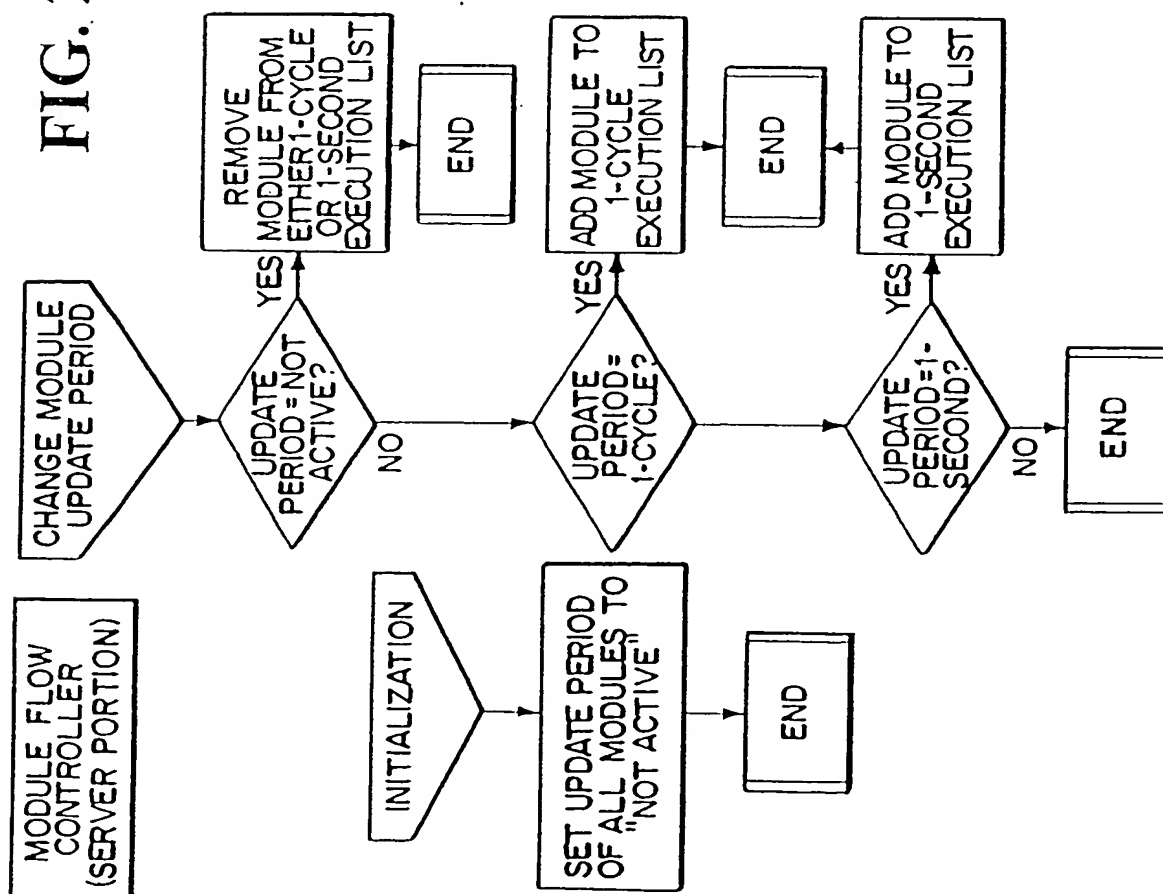


FIG. 24B



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FIG. 25A

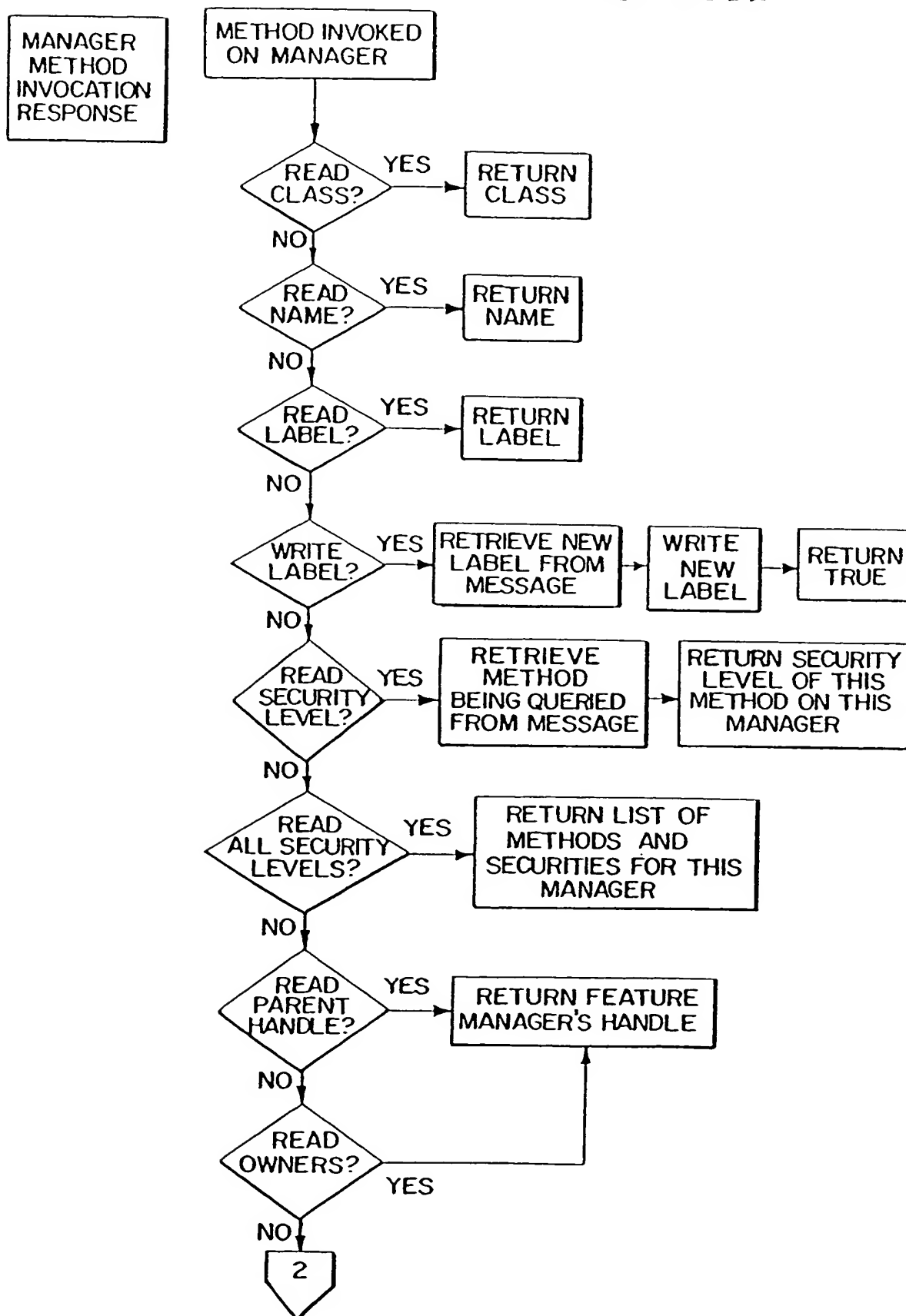


FIG. 25B

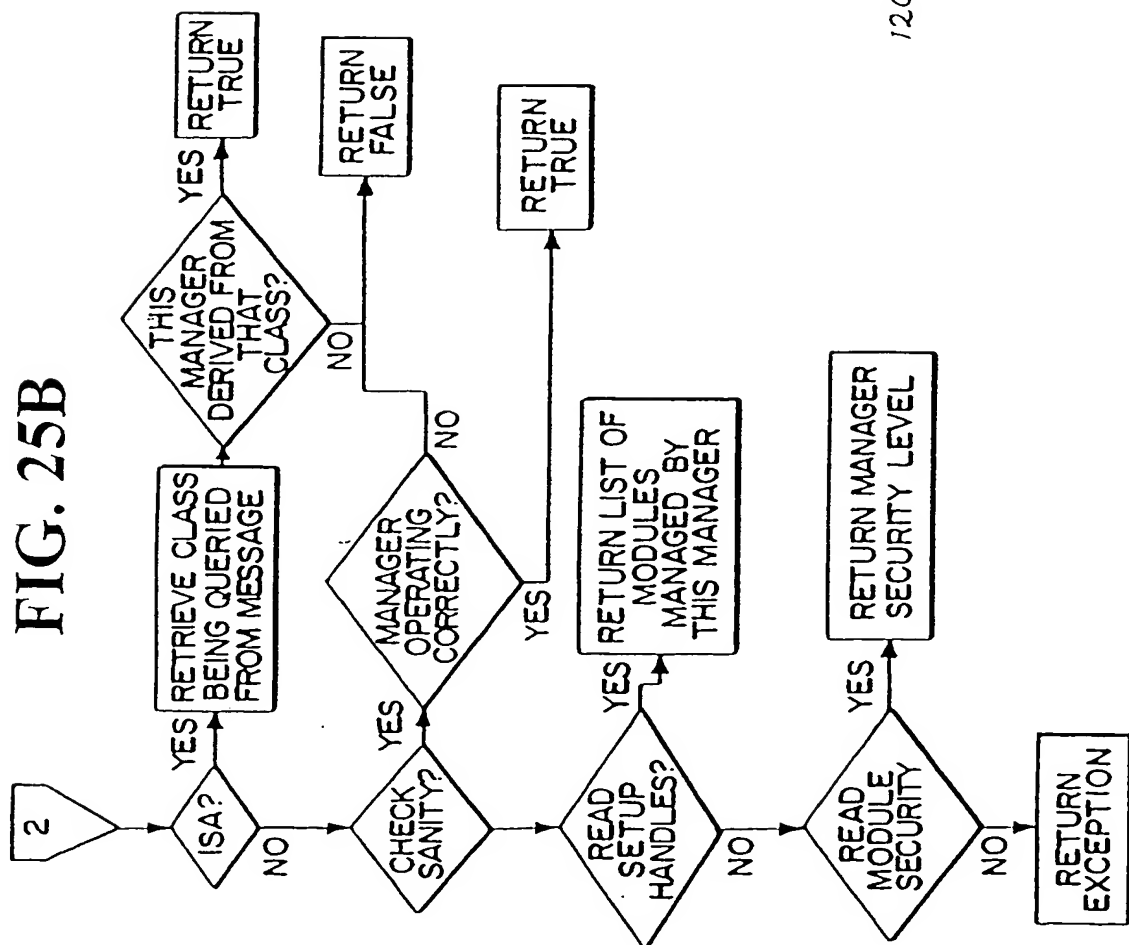


FIG. 26

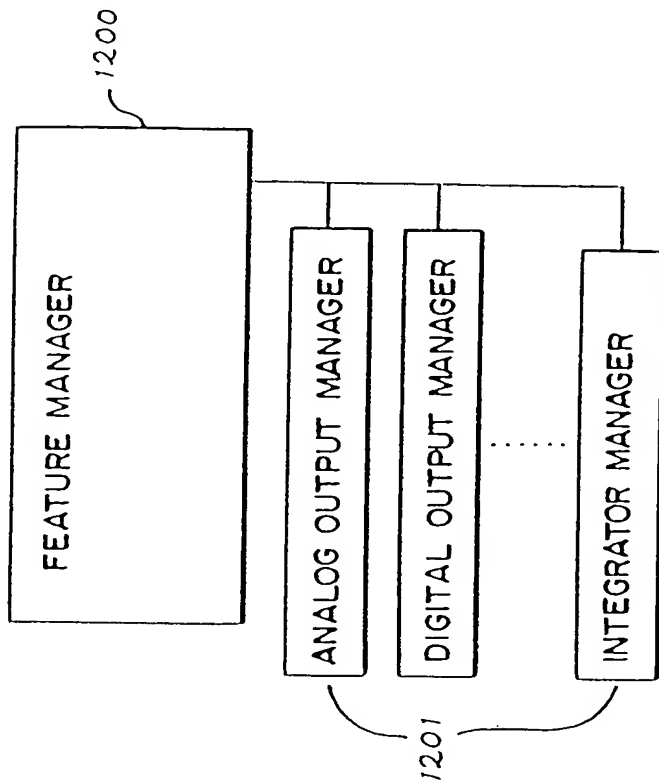




FIG. 26A

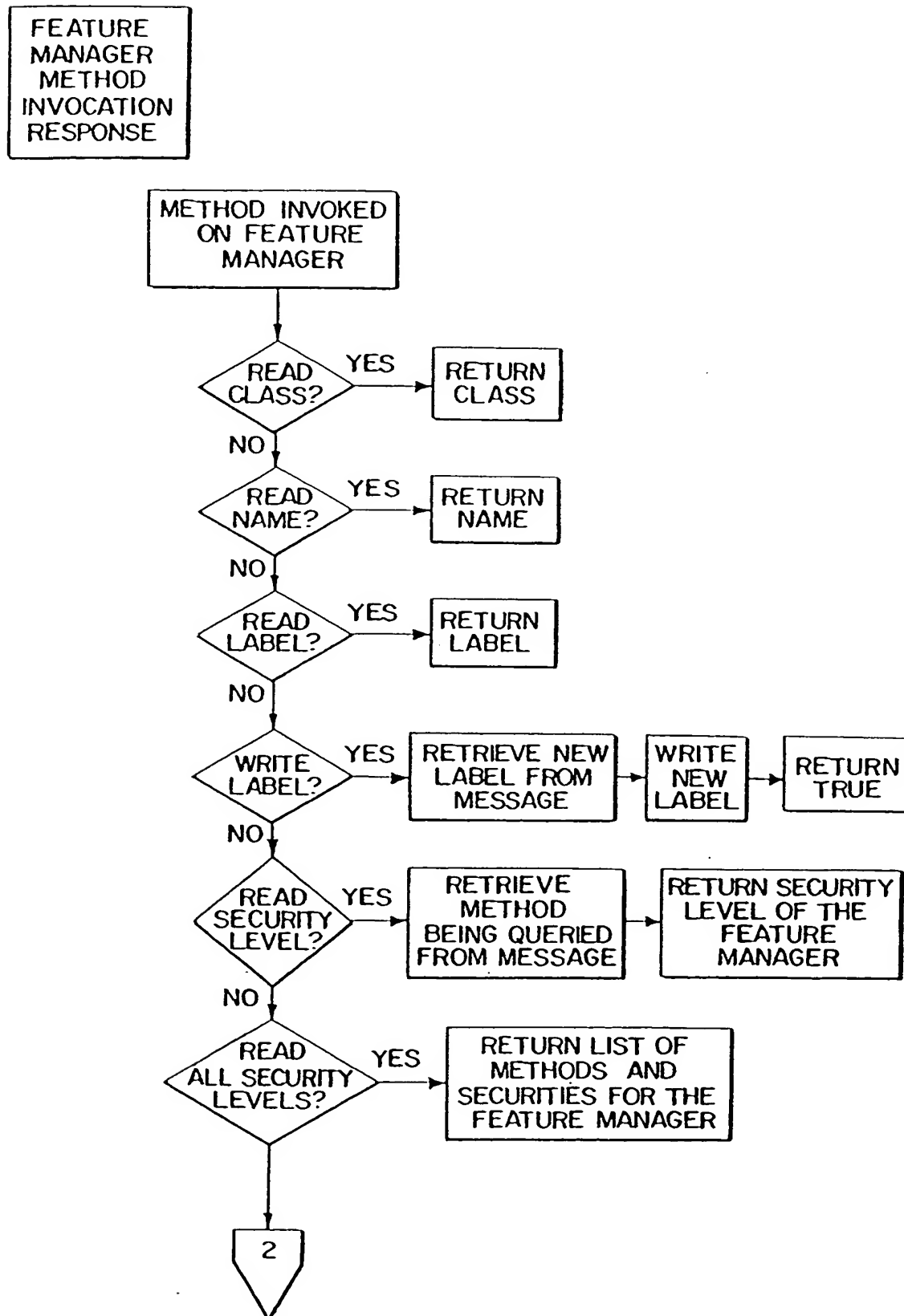
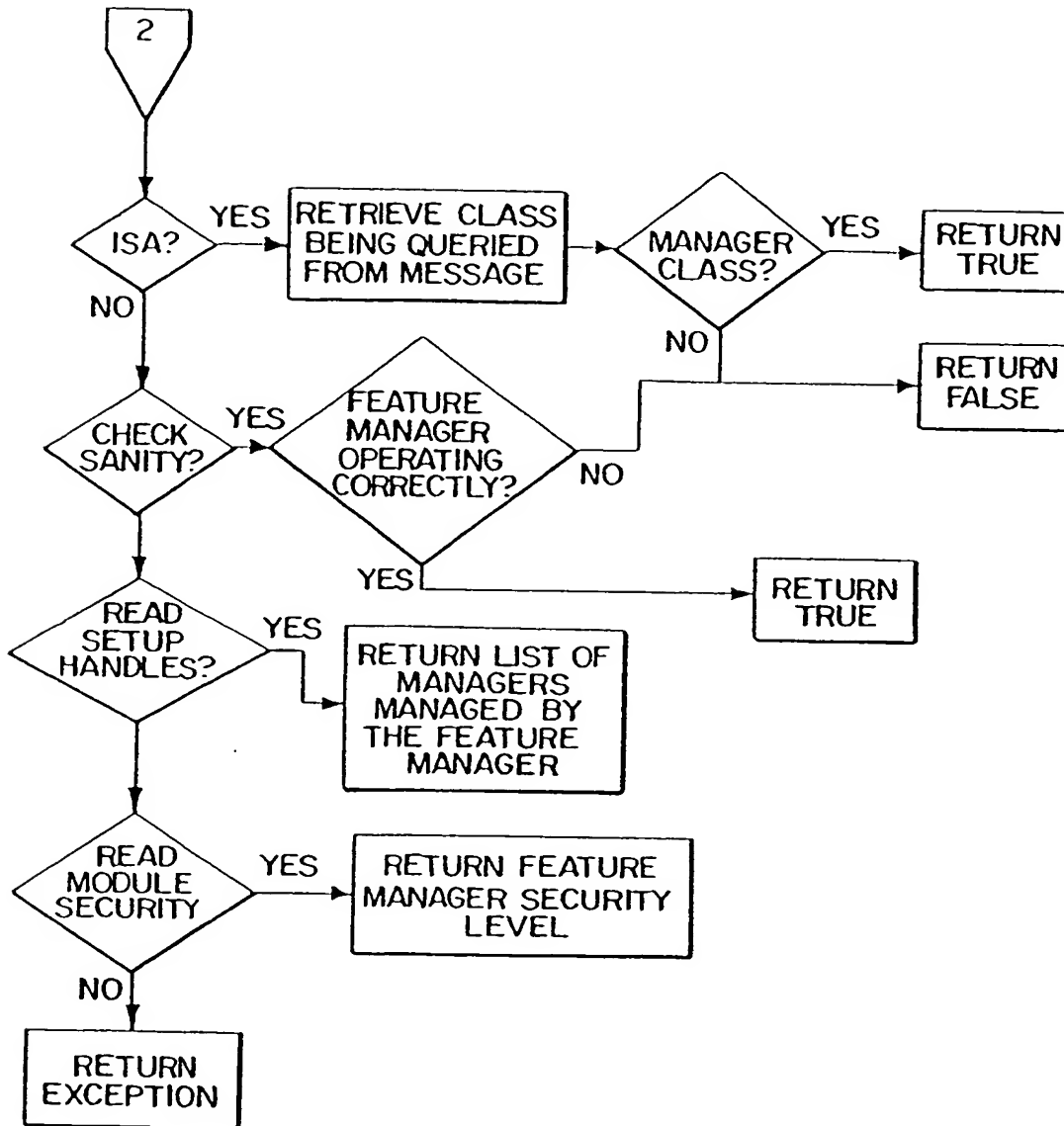


FIG. 26B



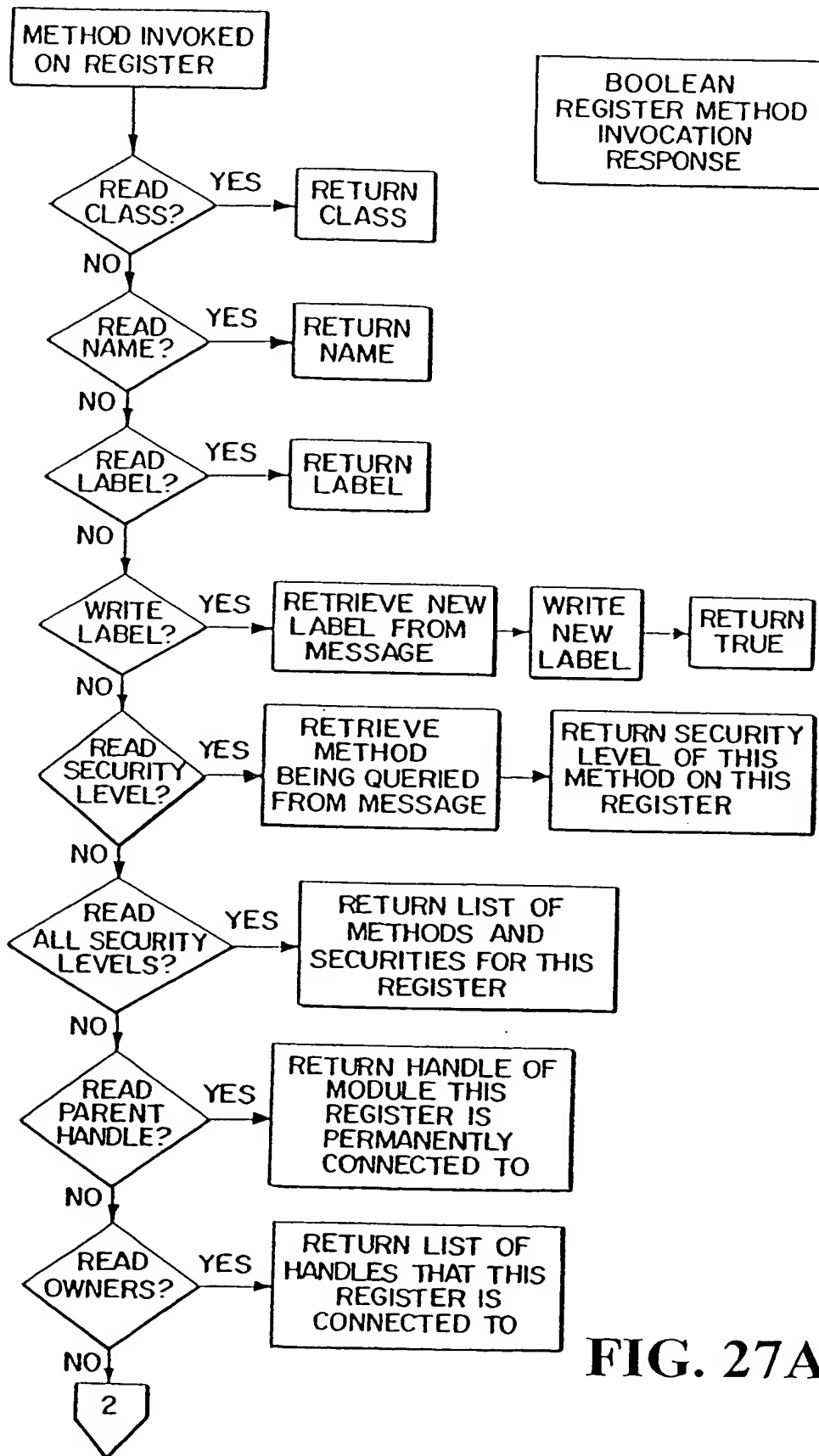


FIG. 27A

FIG. 27B

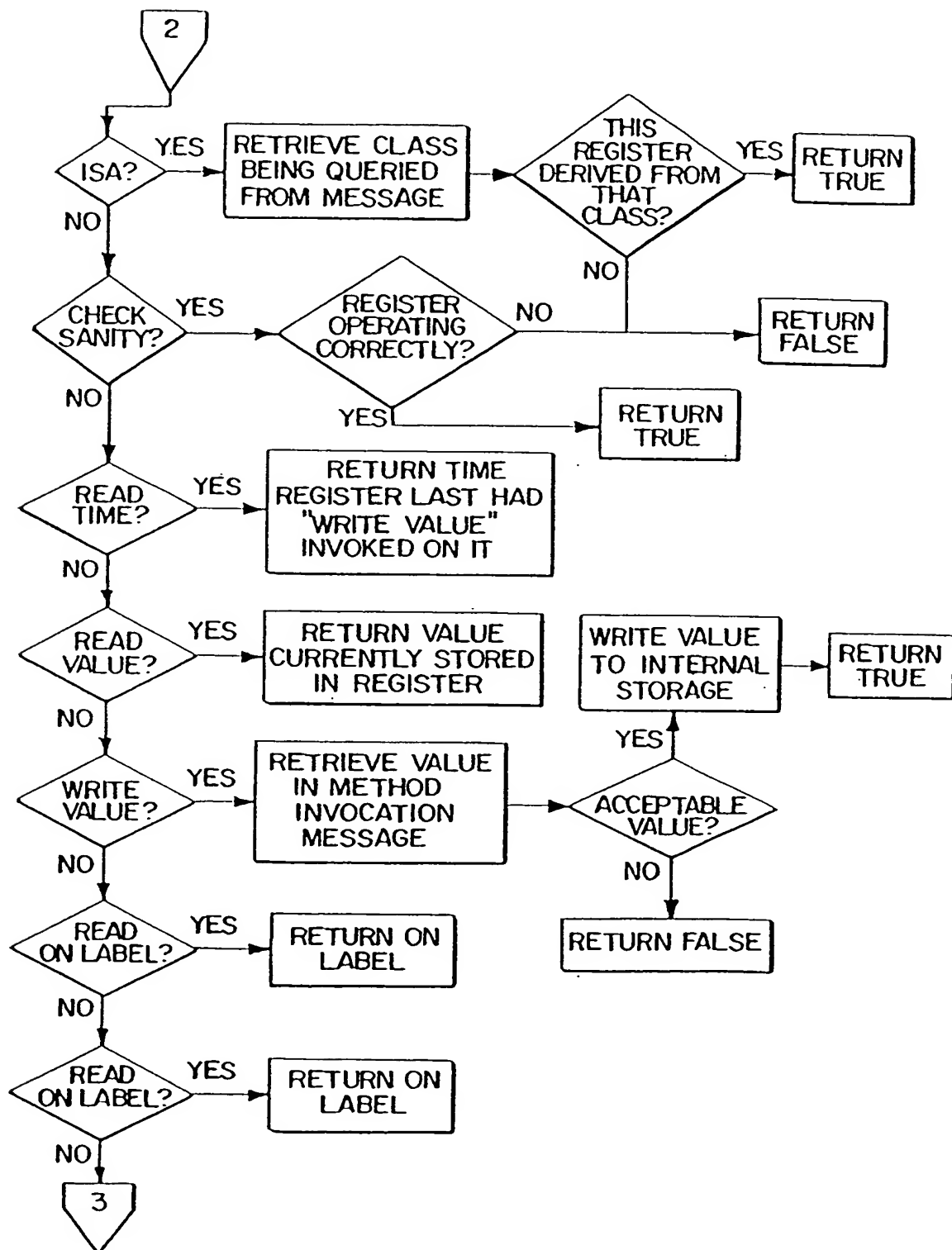


FIG. 27C

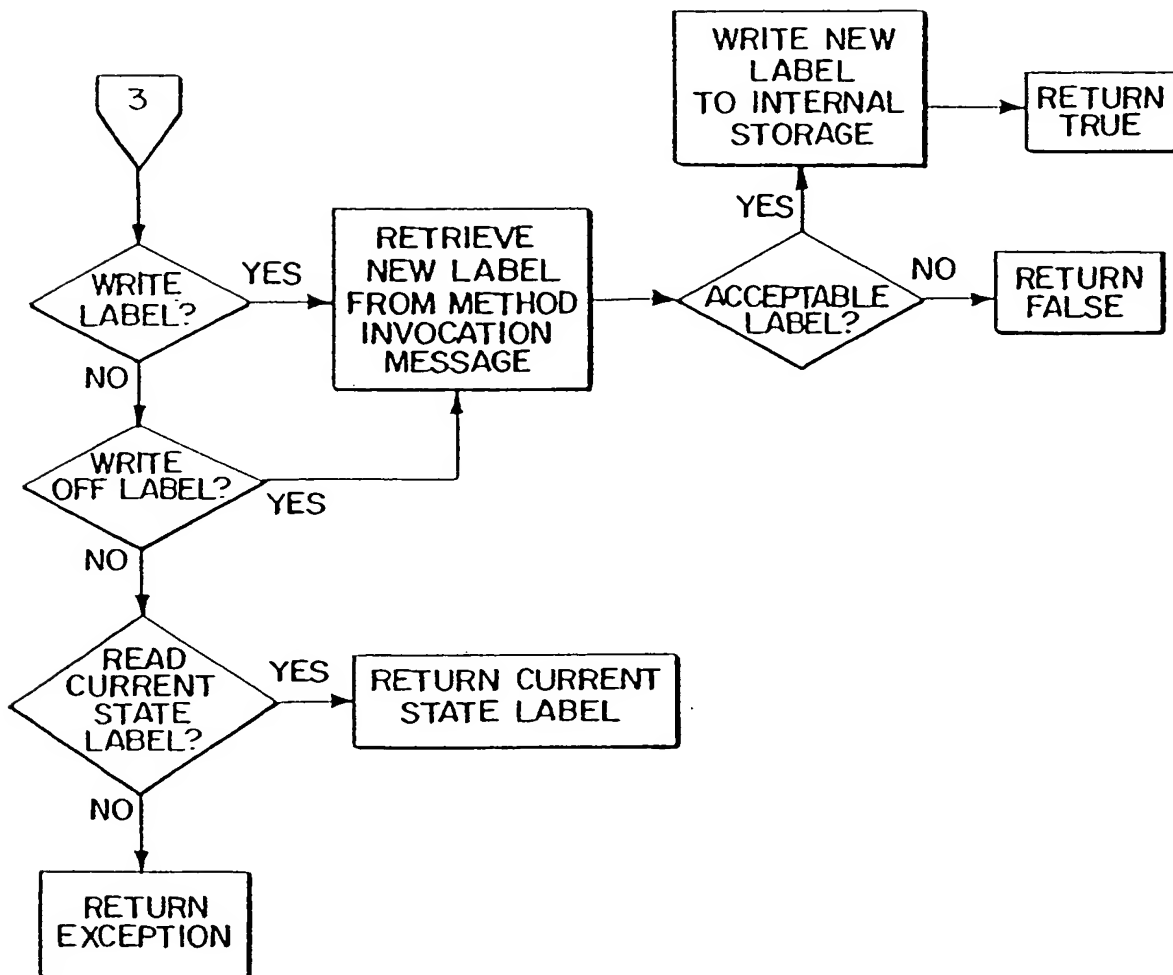


FIG. 28A

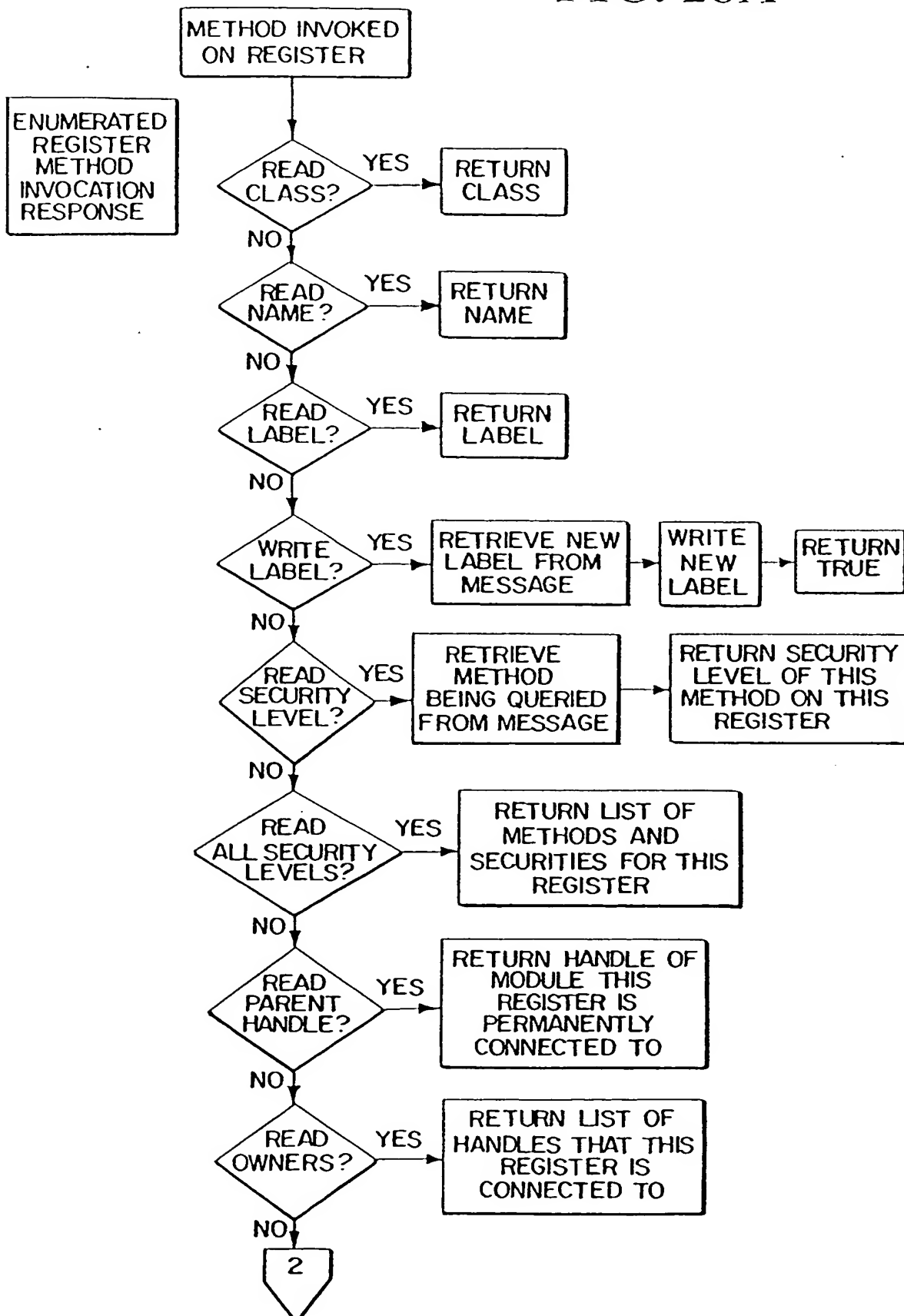


FIG. 28B

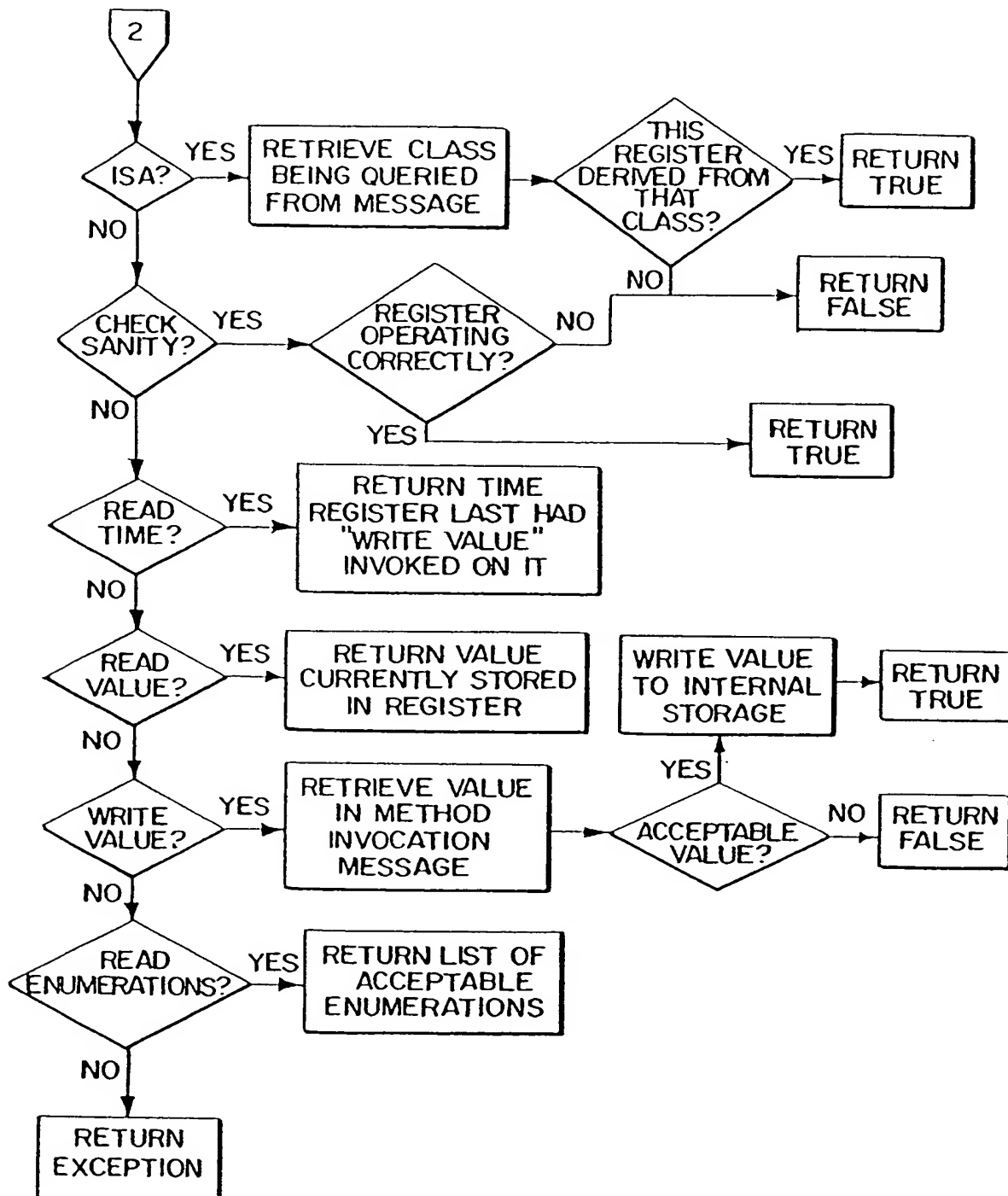
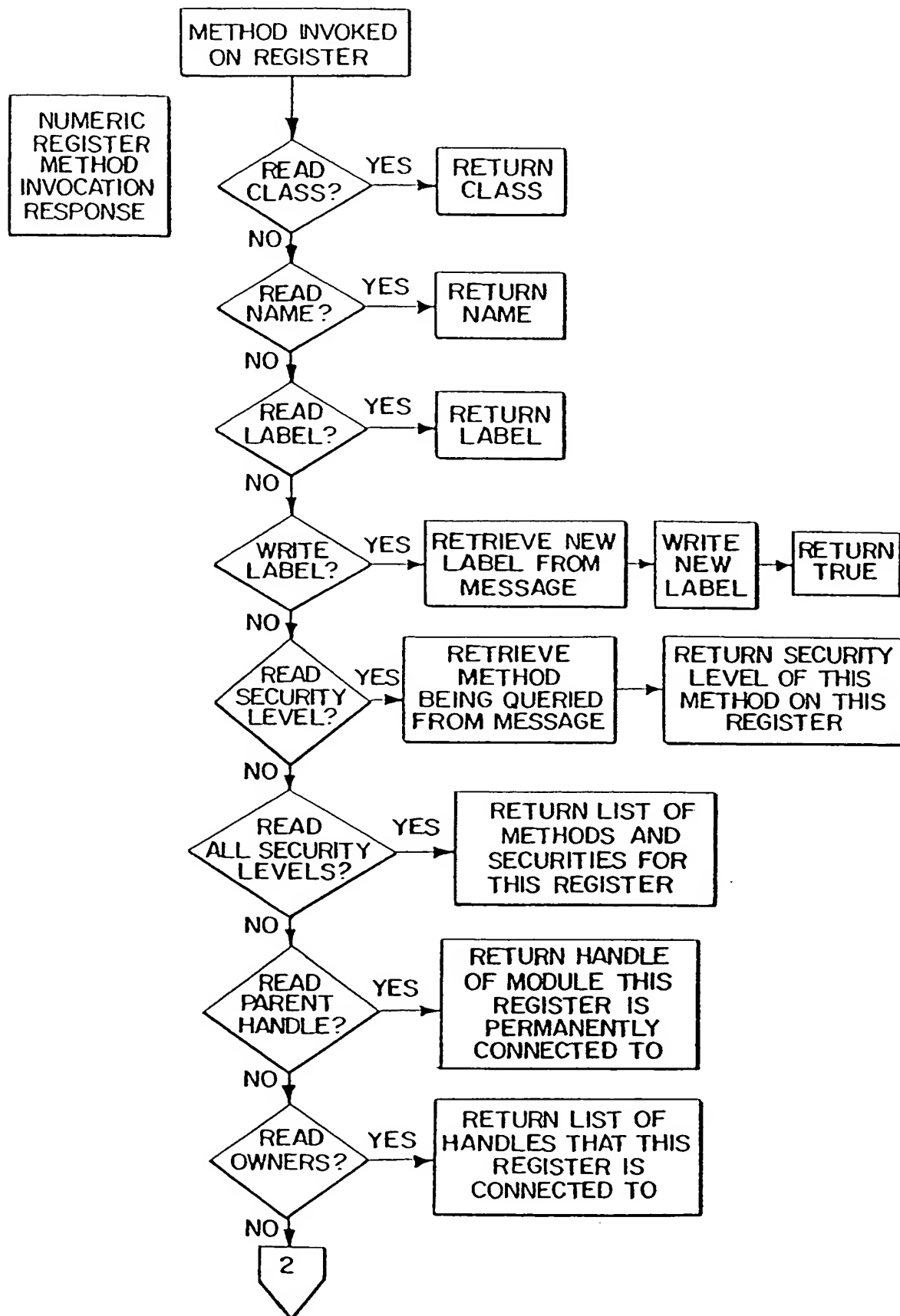


FIG. 29A





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FIG. 29B

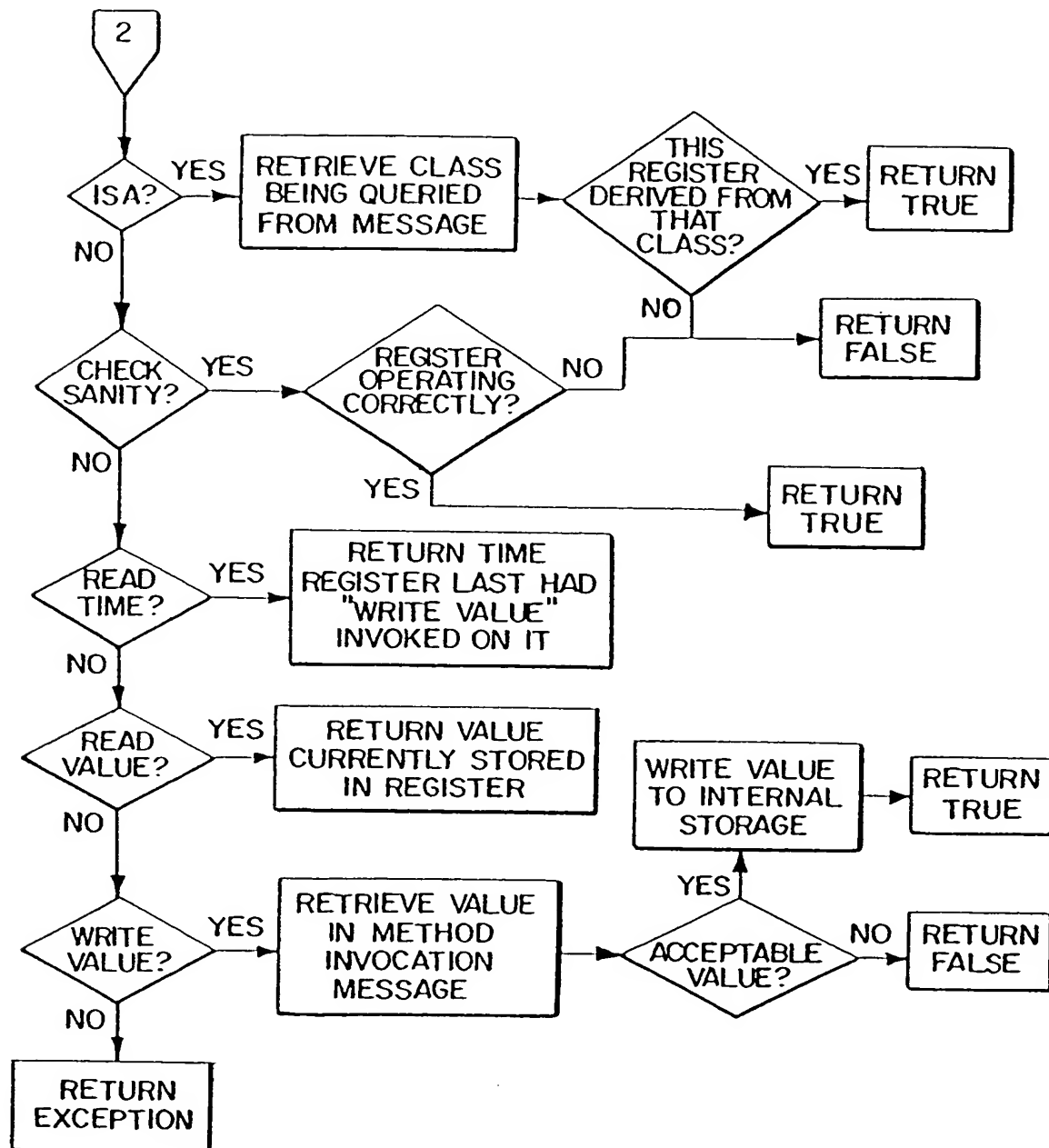


FIG. 30A

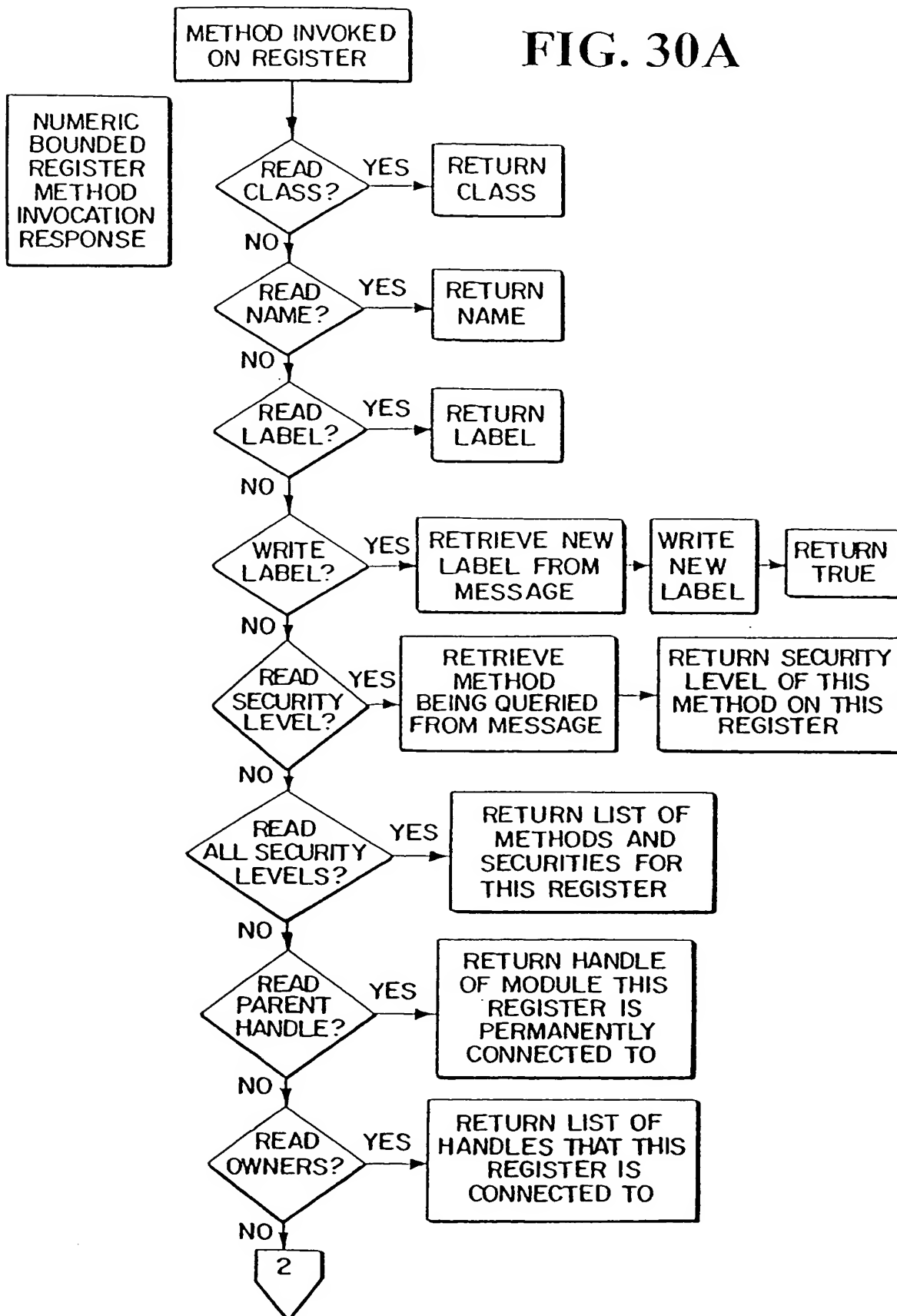
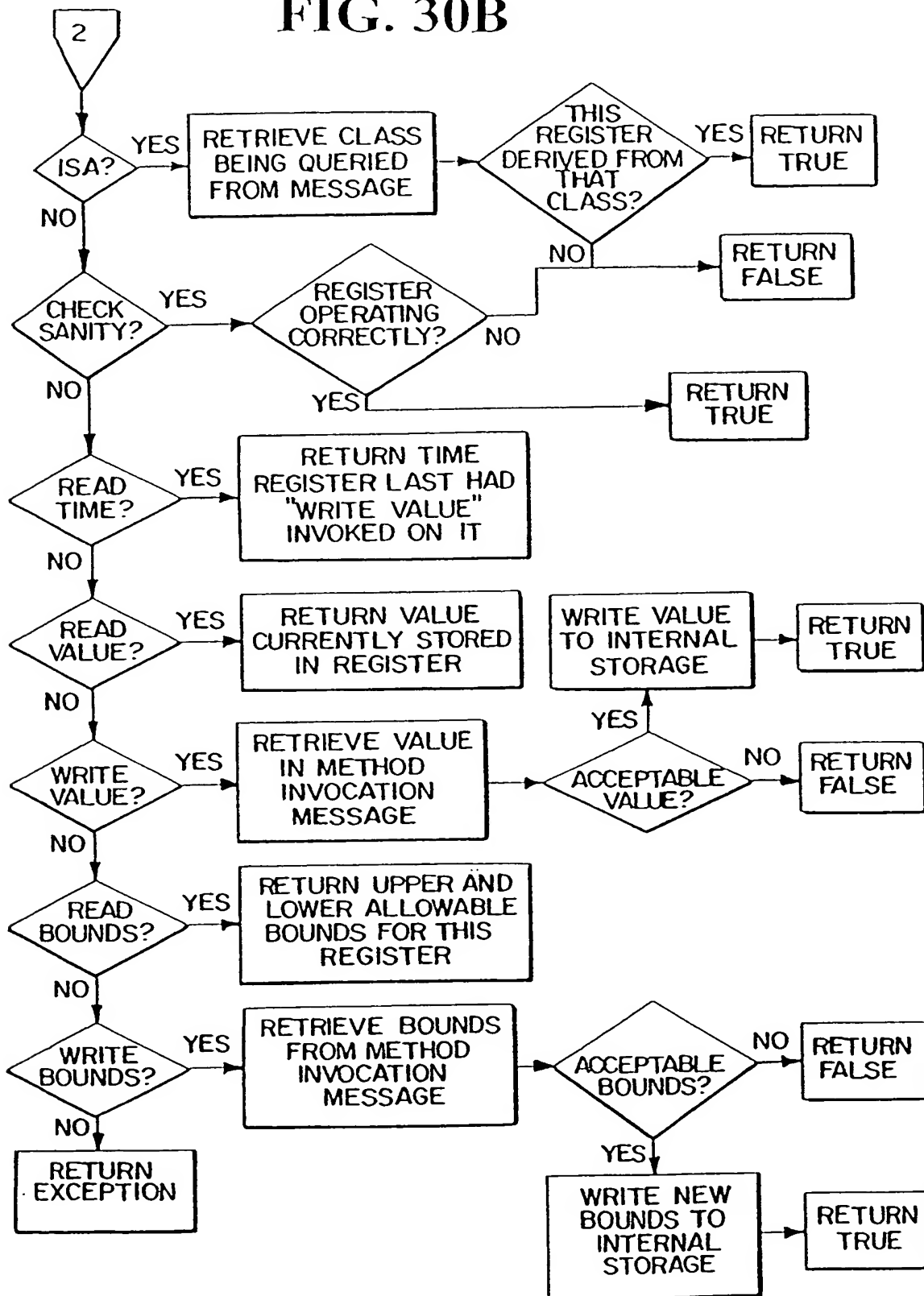


FIG. 30B



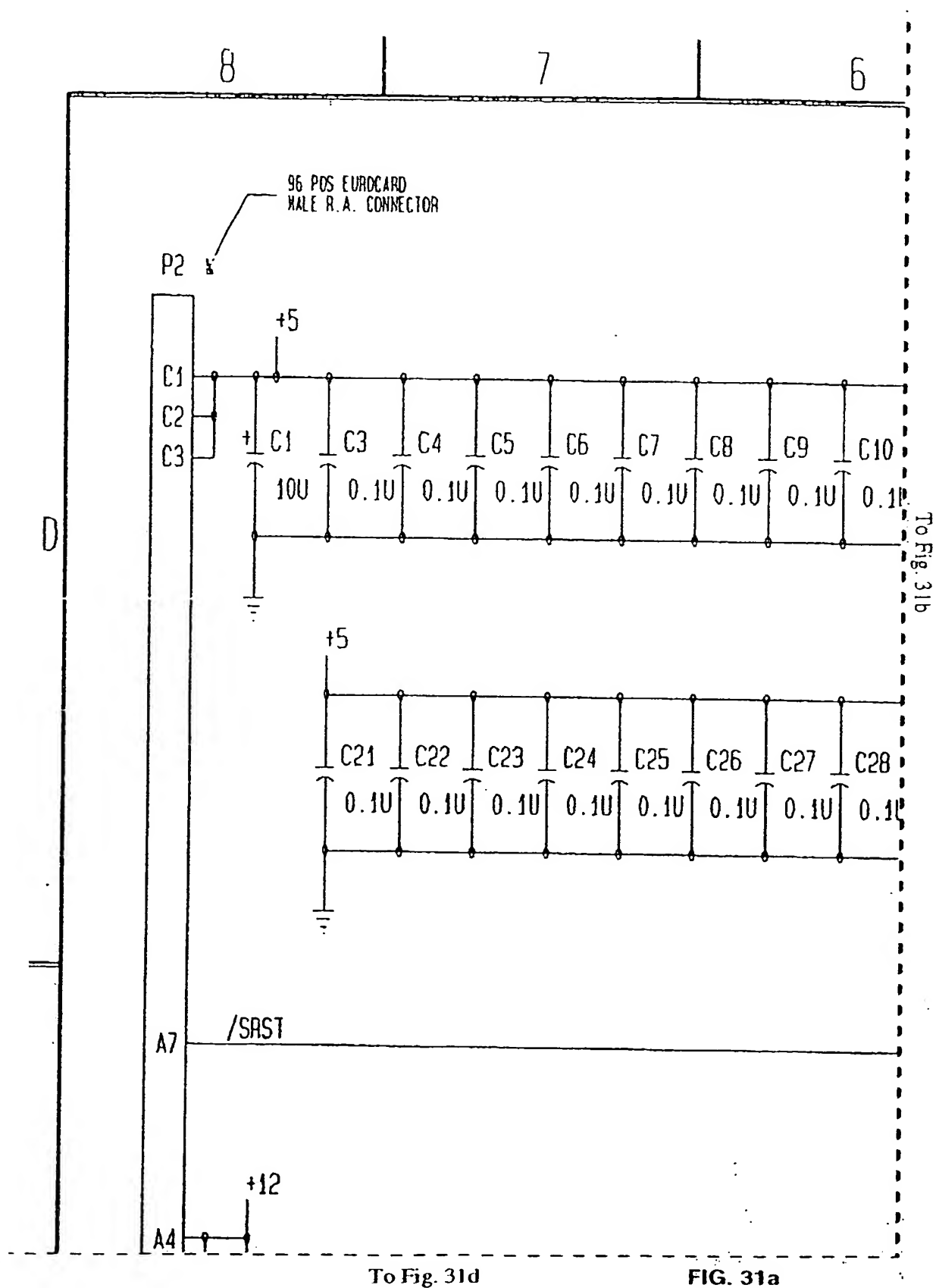
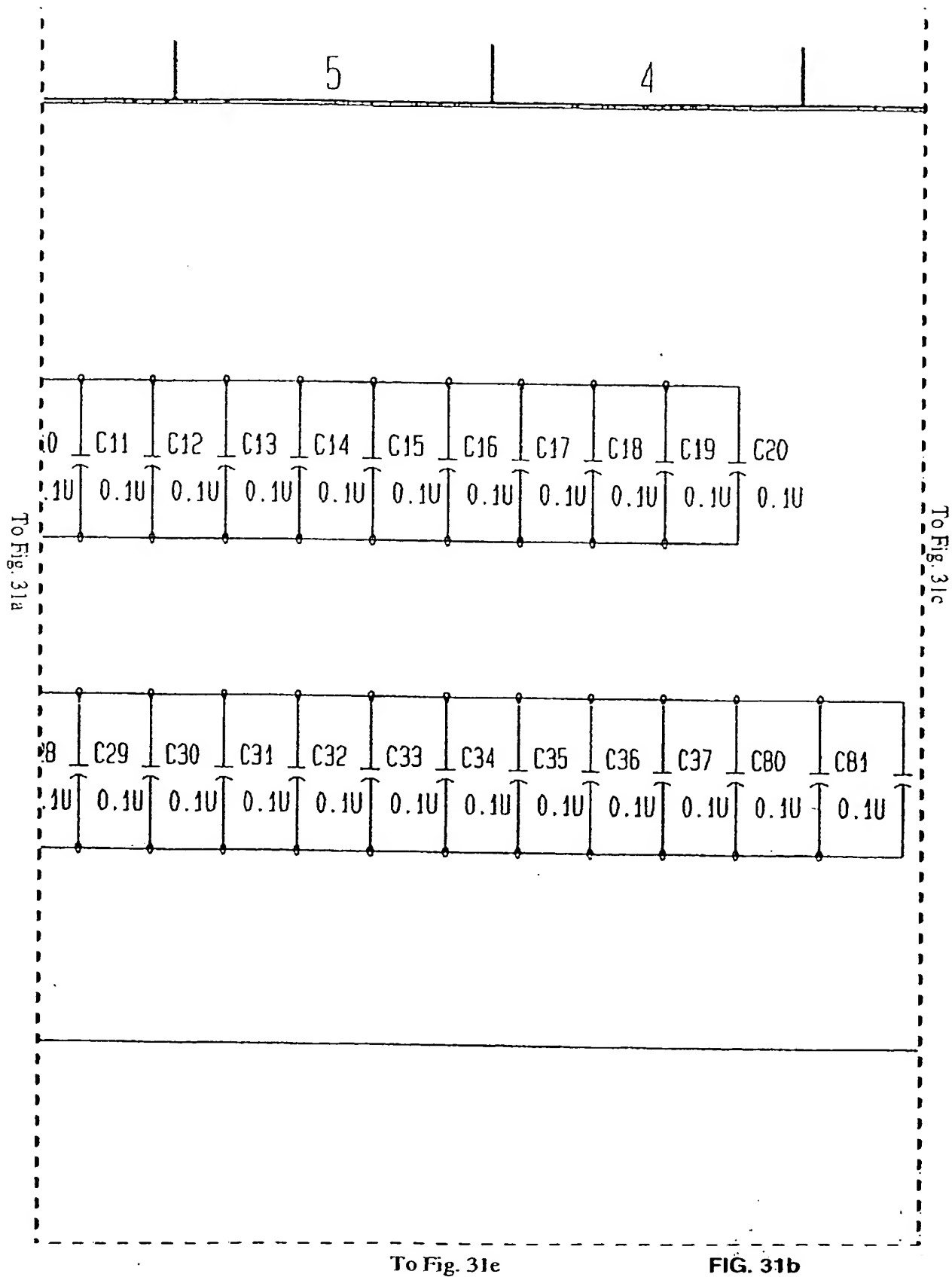
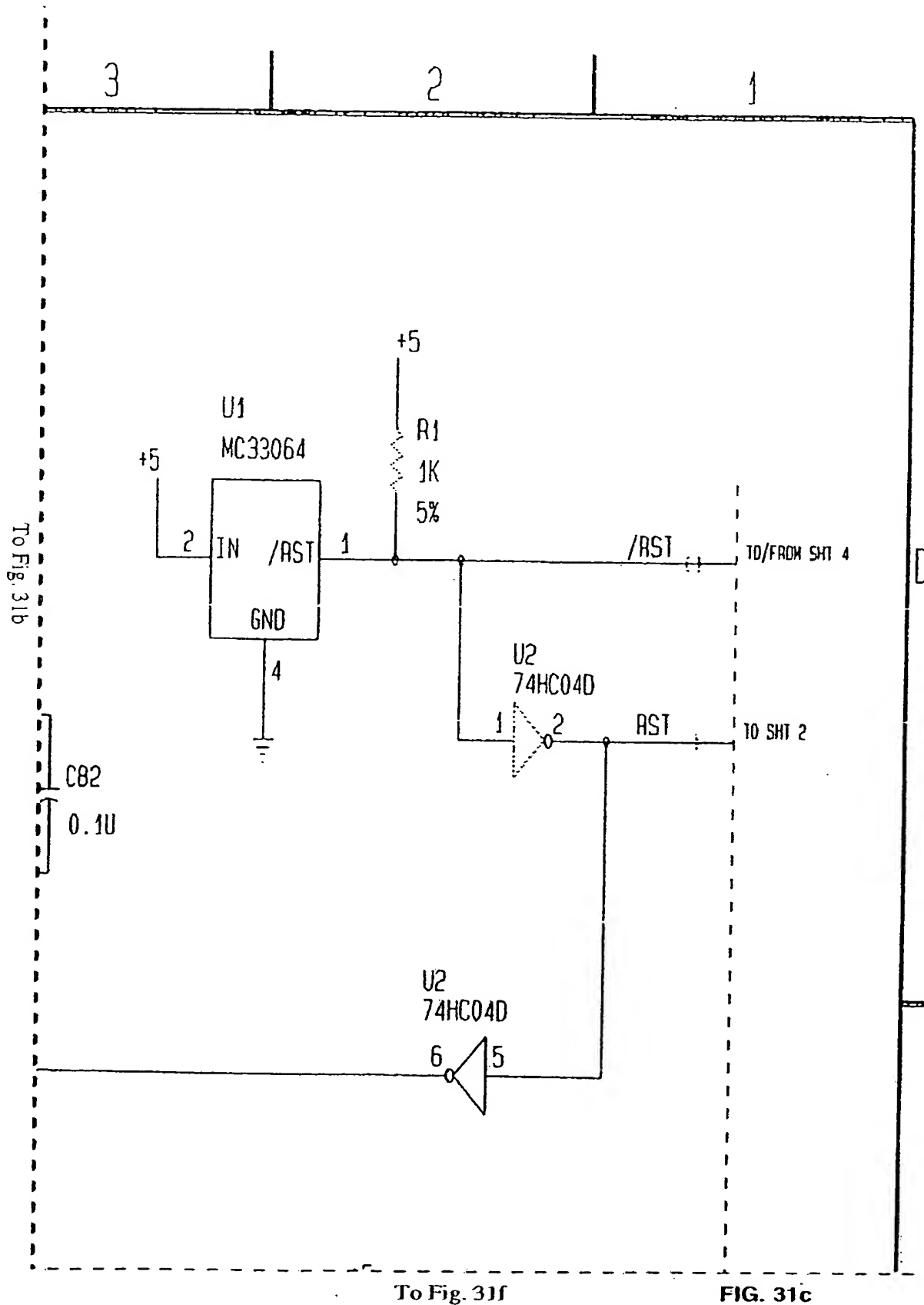


FIG. 31a

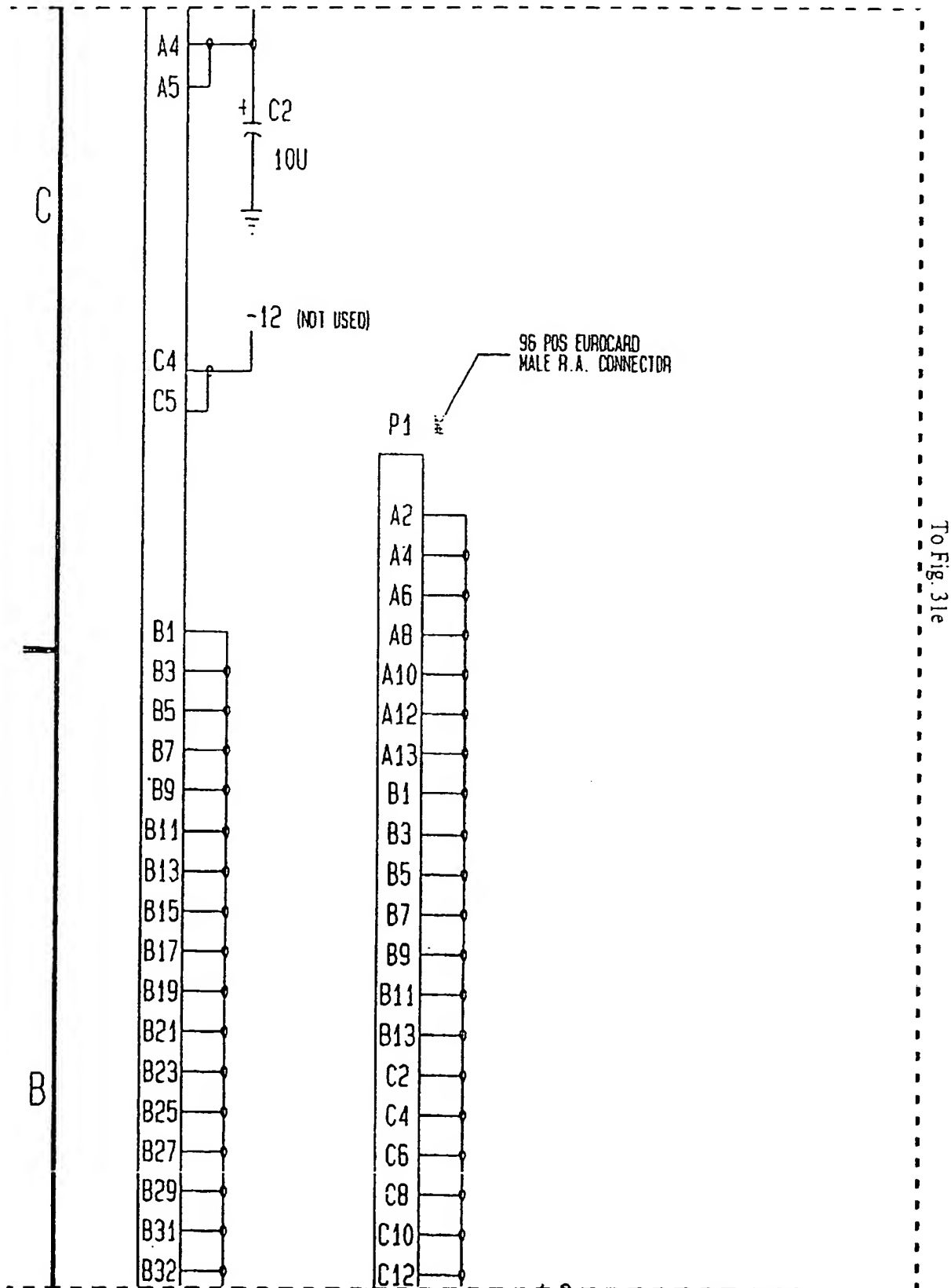


66 96 007



678807

To Fig. 31a



To Fig. 31e

To Fig. 31g

FIG. 31d

68 68207

To Fig. 31b

To Fig. 31d

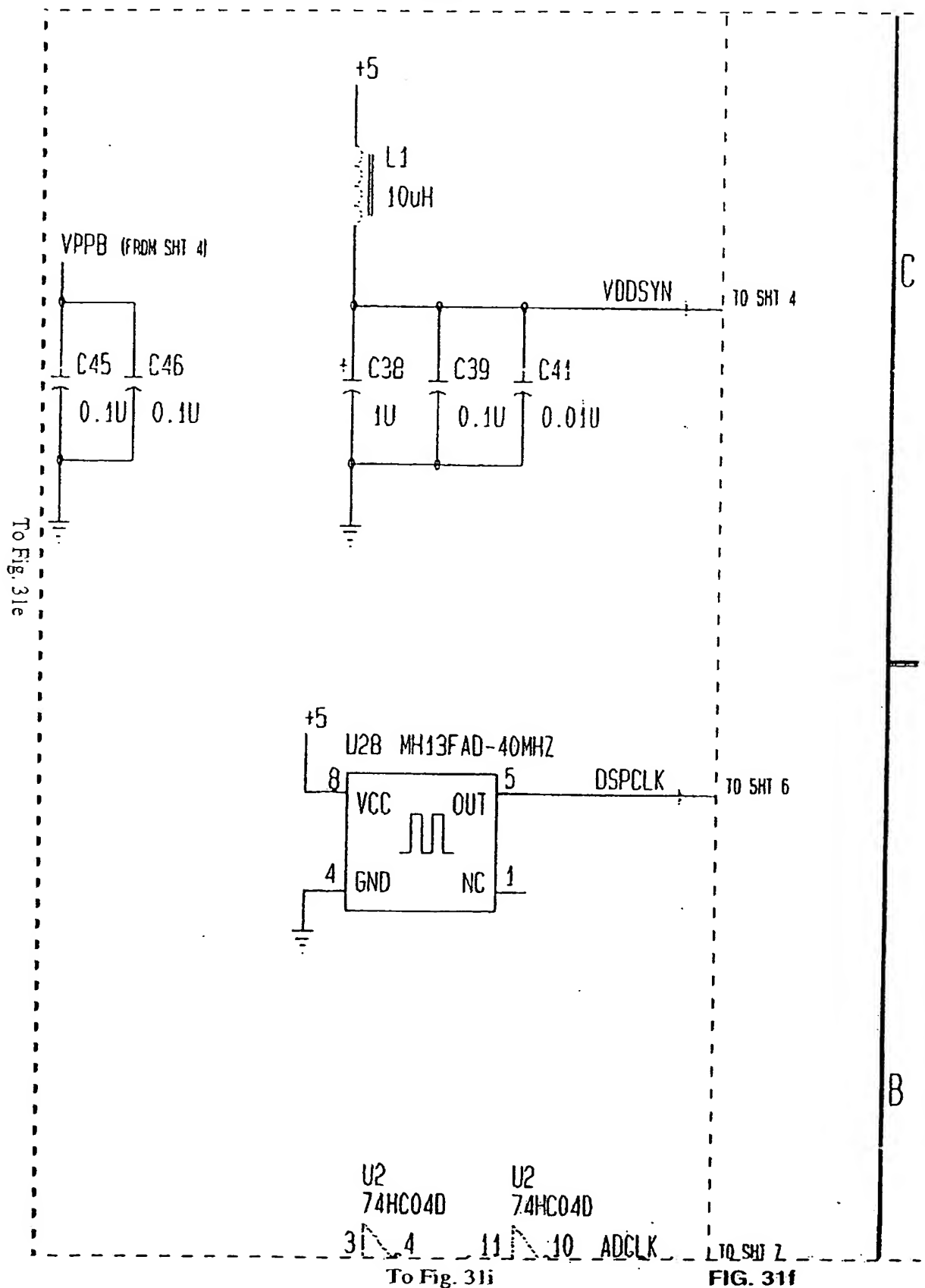
To Fig. 31f

To Fig. 31h

FIG. 31e



To Fig. 31c

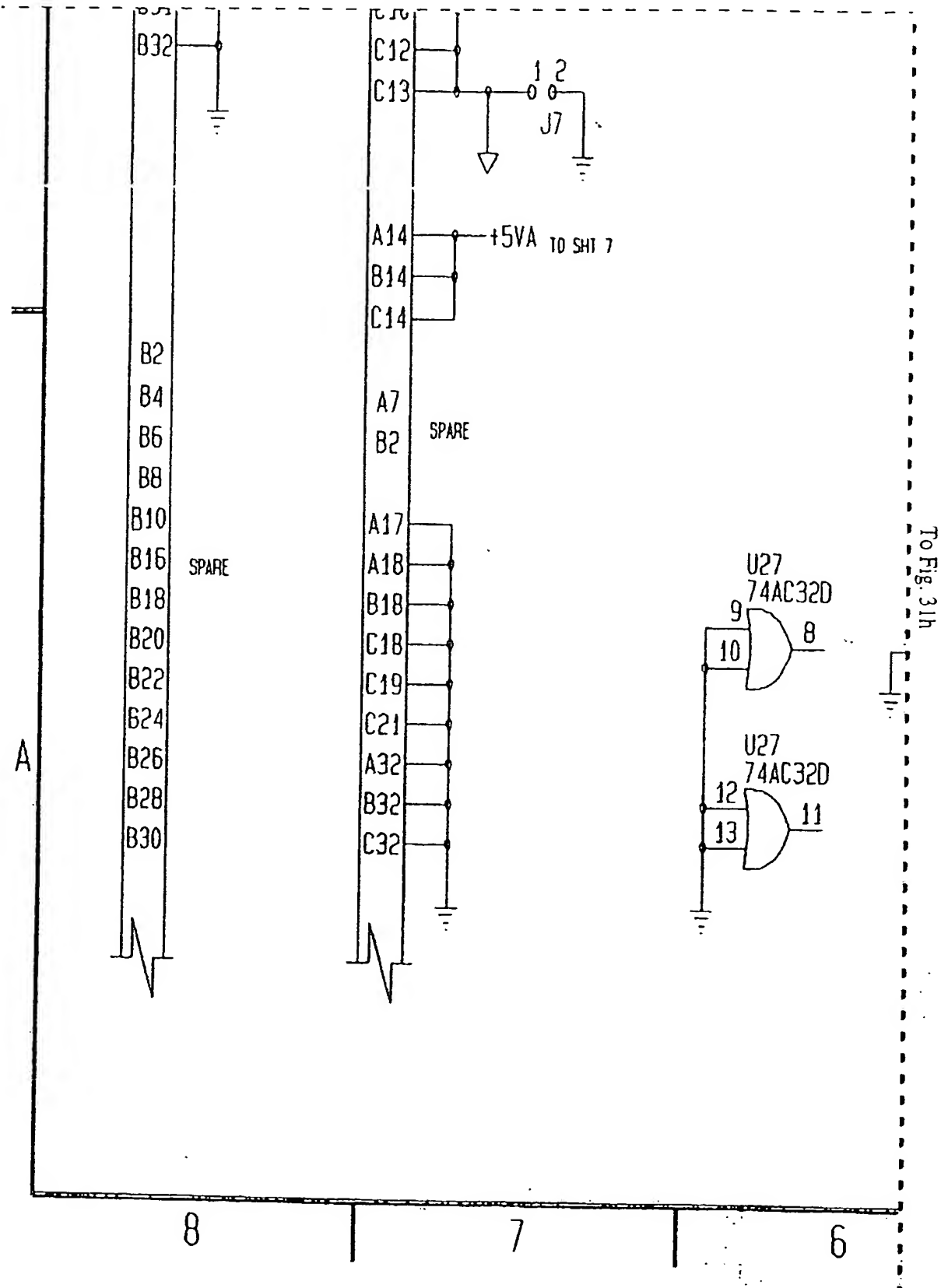


To Fig. 31i

FIG. 31f

7063-07

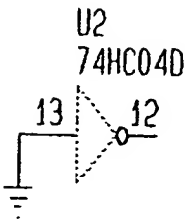
To Fig. 31d



71 68 207

To Fig. 31e

To Fig. 31g



To Fig. 31i

This schematic  
proprietary  
configuration  
are issued in  
or use shall  
of CD Power M

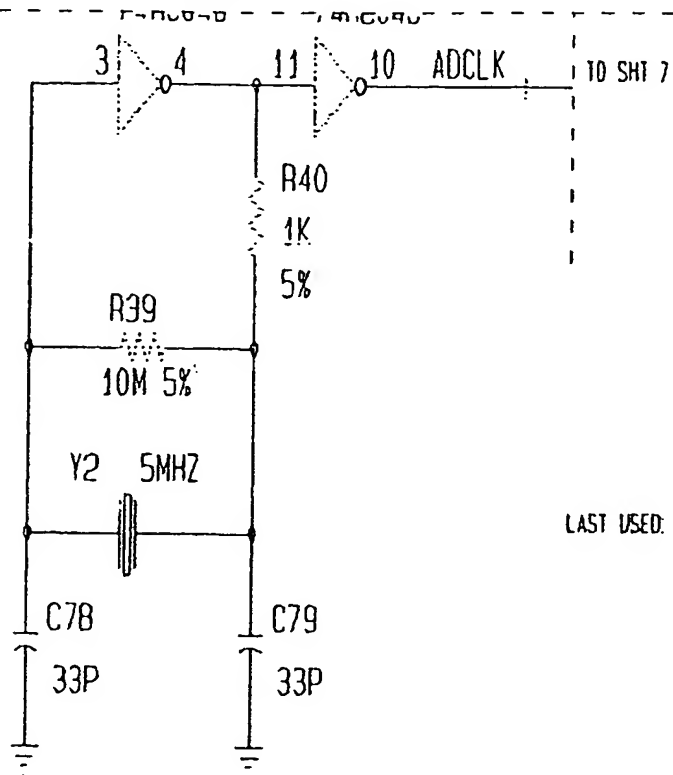
5

4

FIG. 31h

72 96 207

To Fig. 31f



LAST USED: C83  
R62  
U28  
P3  
J17  
TP11  
DS2

To Fig. 31h



POWER MEASUREMENT LTD.

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of Power Measurement Ltd.

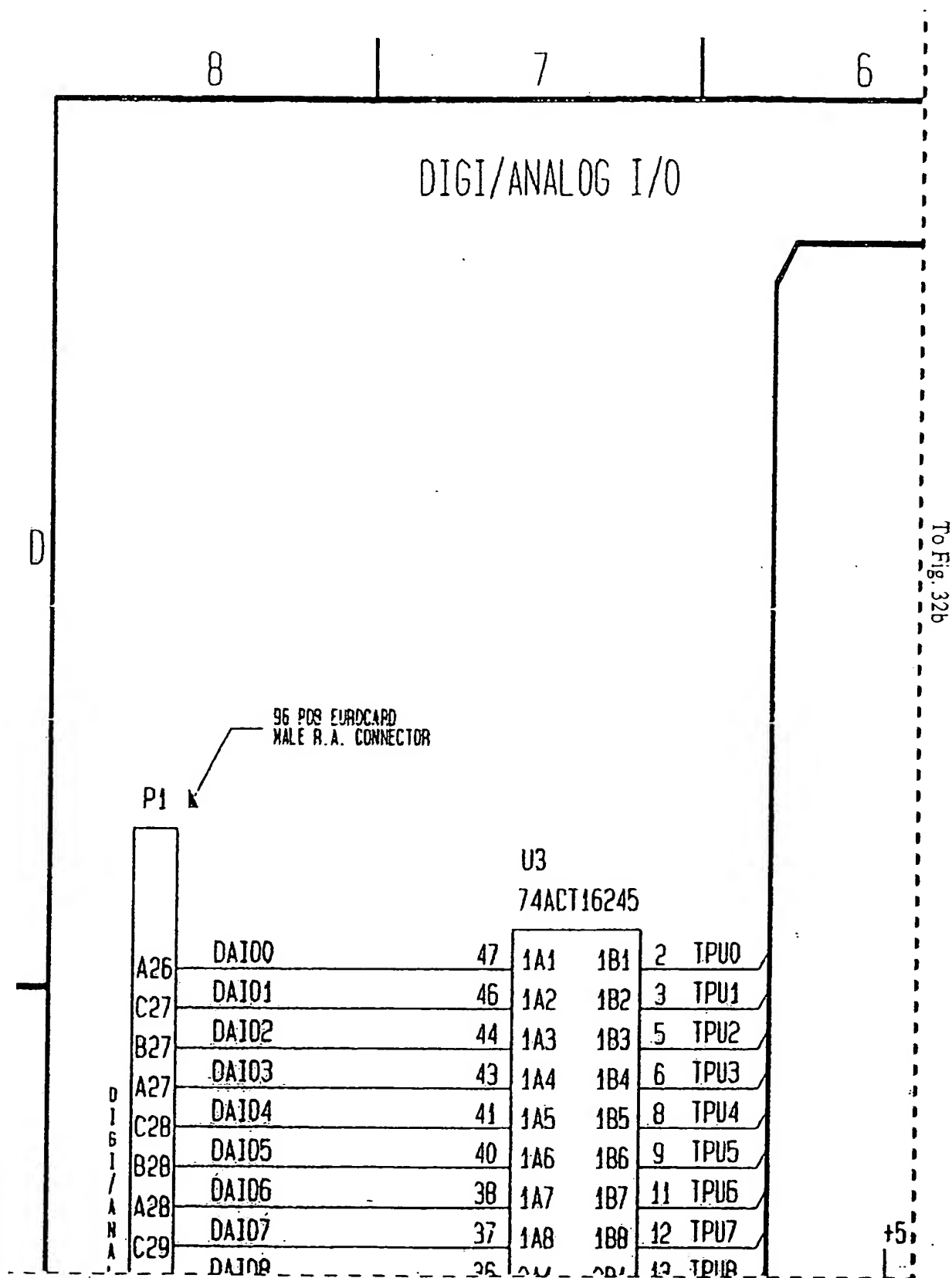
E			REV 1.2
DATE: MAY 20, 1993		SHEET 1 OF 7	

3

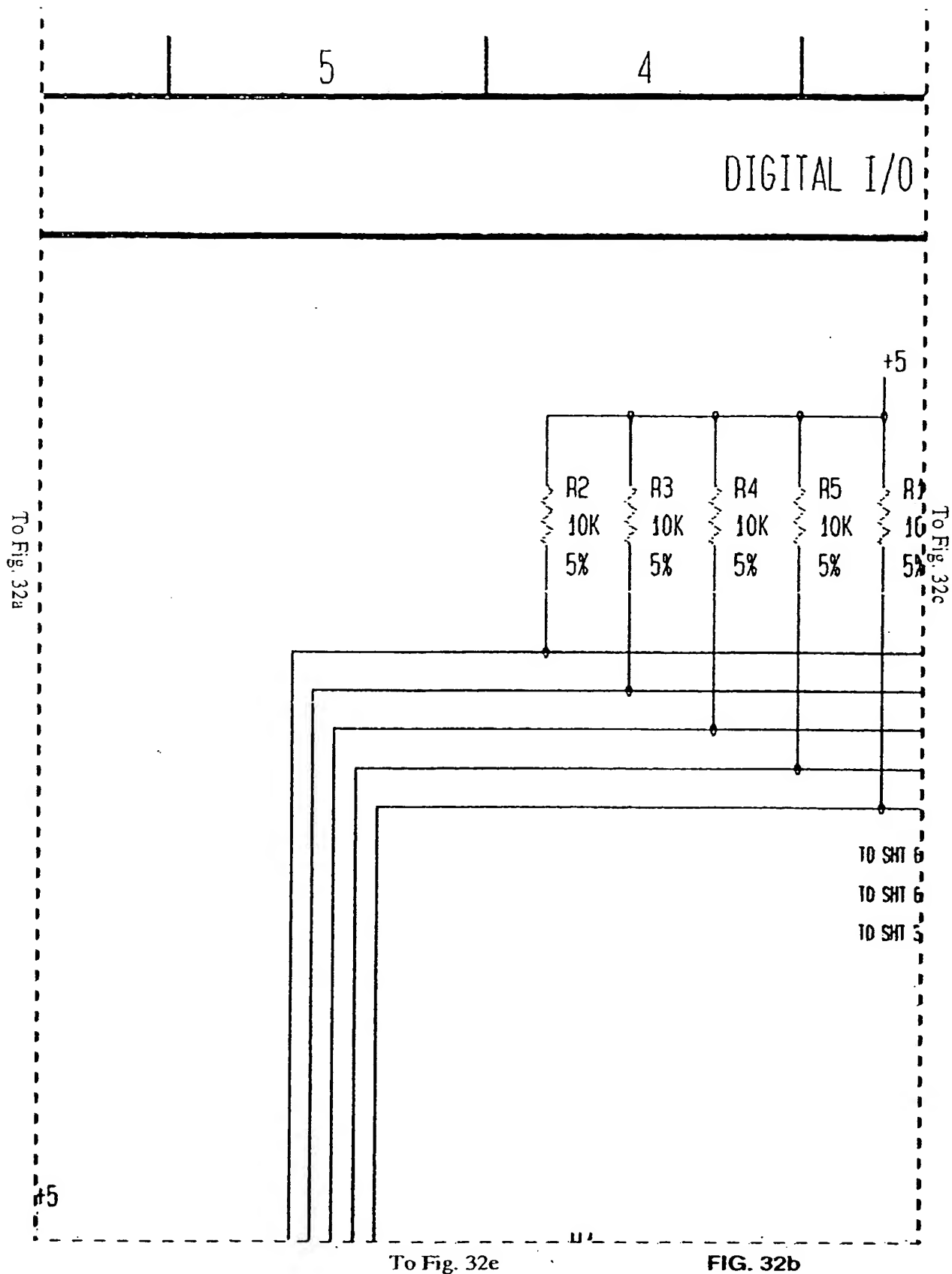
2

1

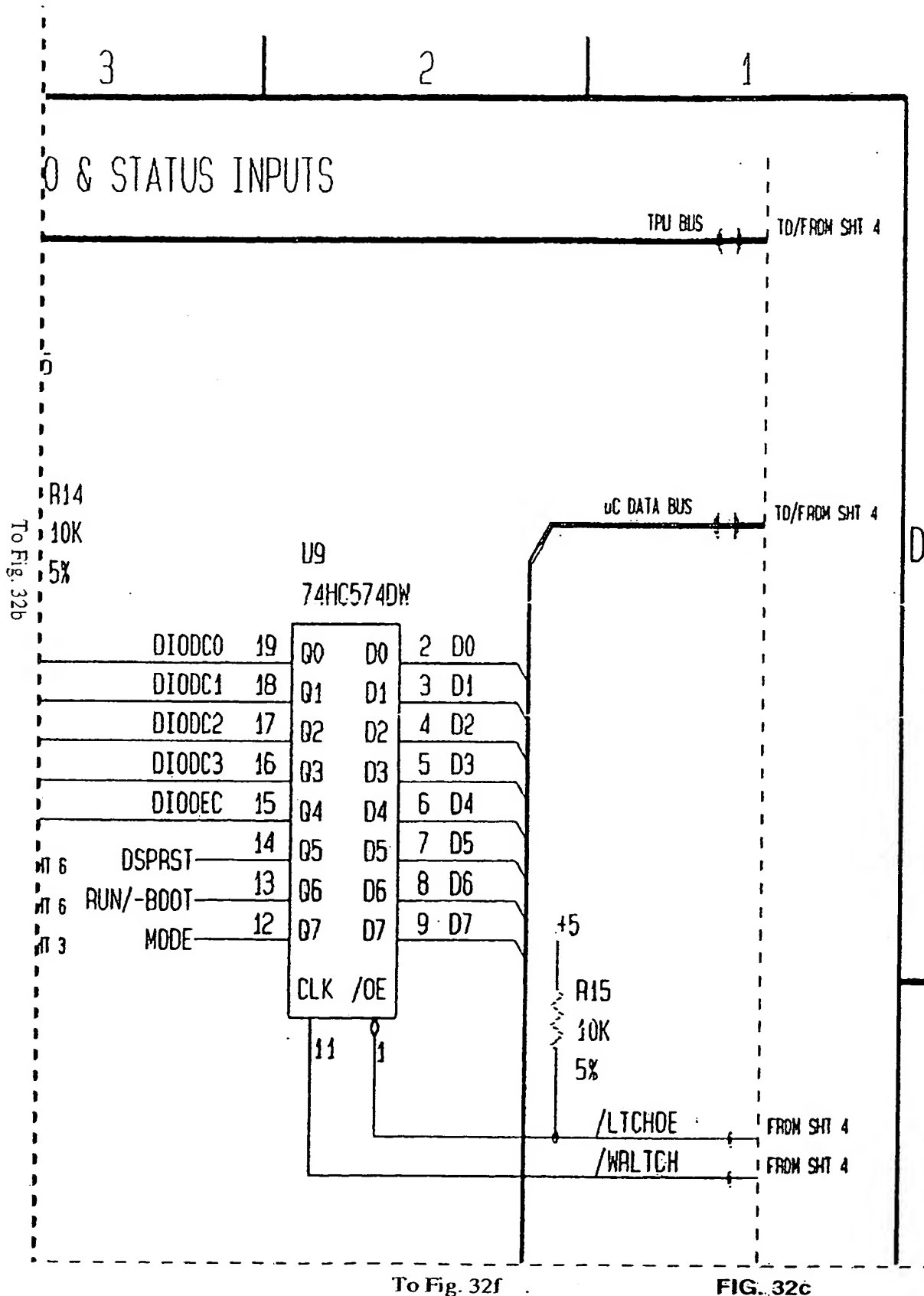
FIG. 31i



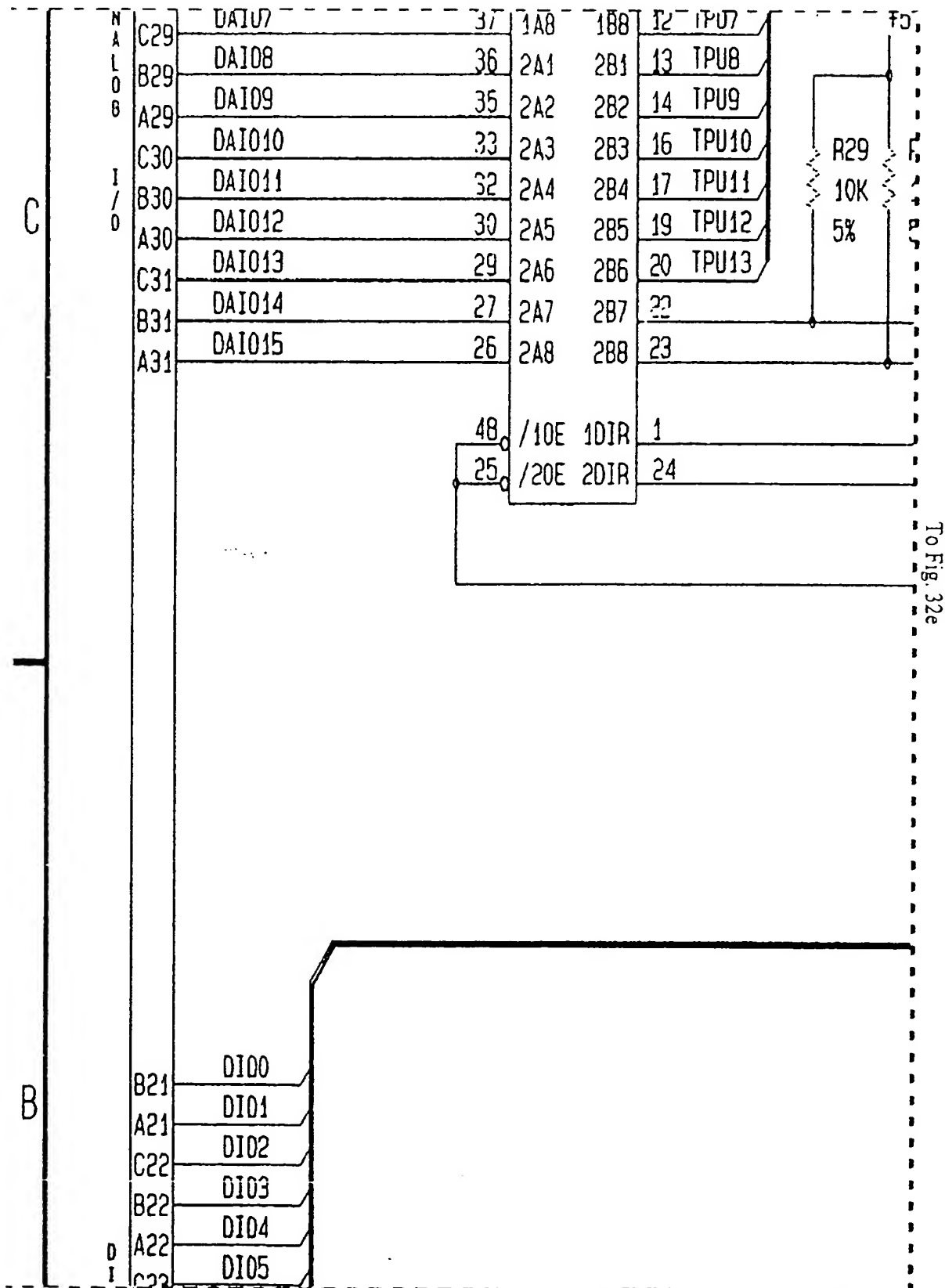
14 66 207



76 8 207



To Fig. 32a



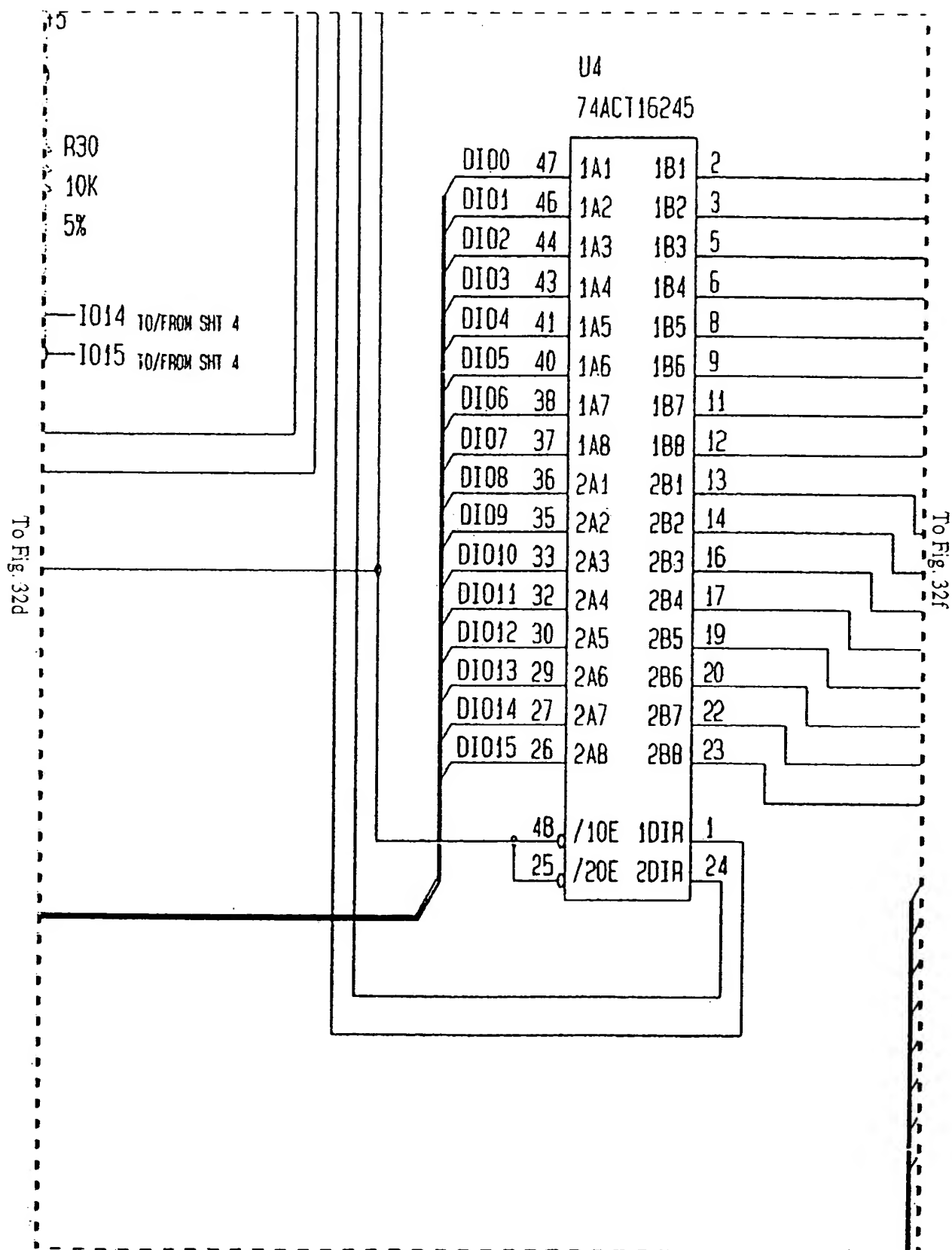
To Fig. 32g

FIG. 32d



77 06 207

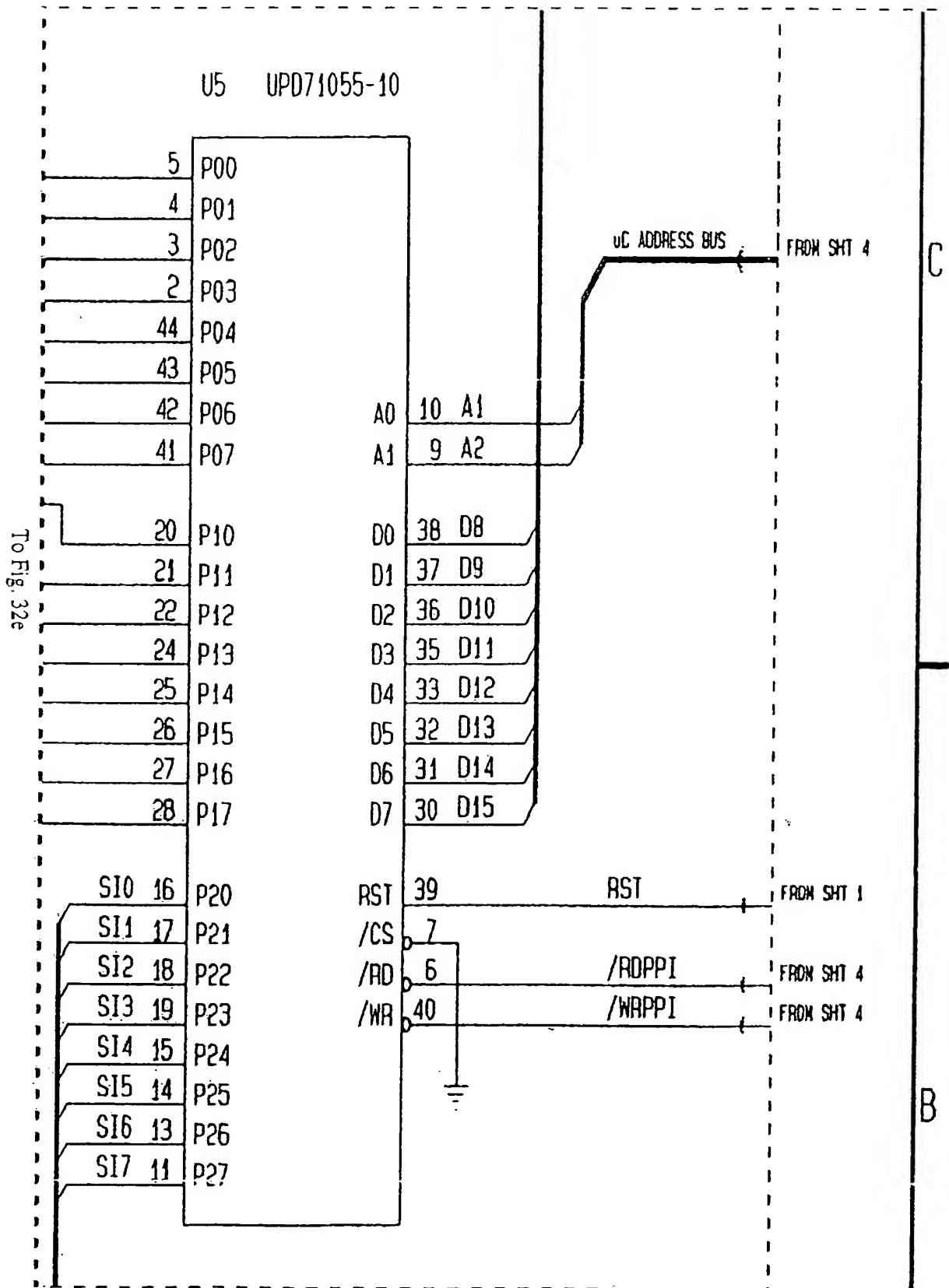
To Fig. 32b



To Fig. 32h

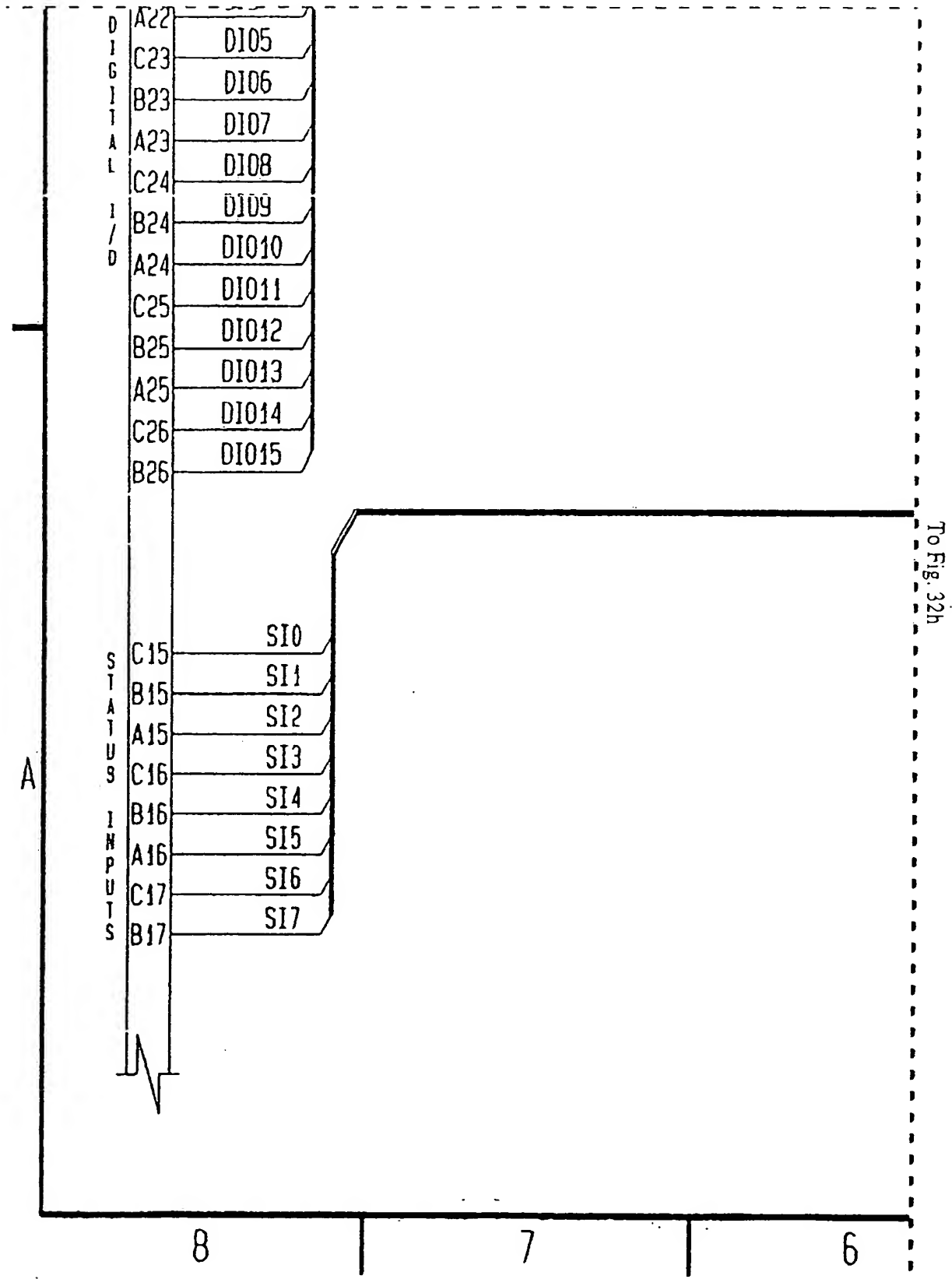
FIG. 32e

To Fig. 32c



79 8 207

To Fig. 32d



To Fig. 32h

FIG. 32g

8c 07 207

To Fig. 32c

To Fig. 32g

To Fig. 32i

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FIG. 32h

To Fig. 32f

To Fig. 32h

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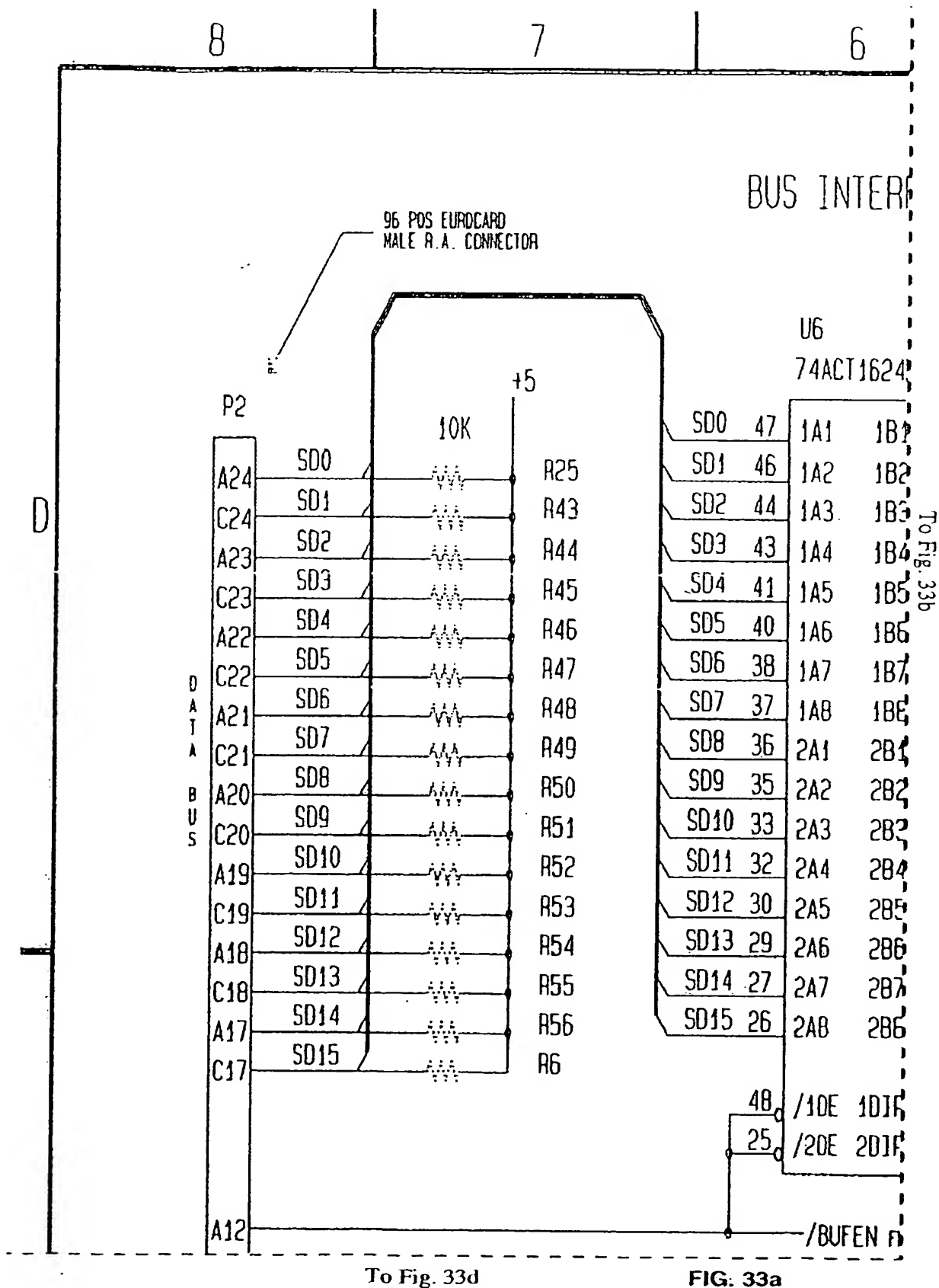
3

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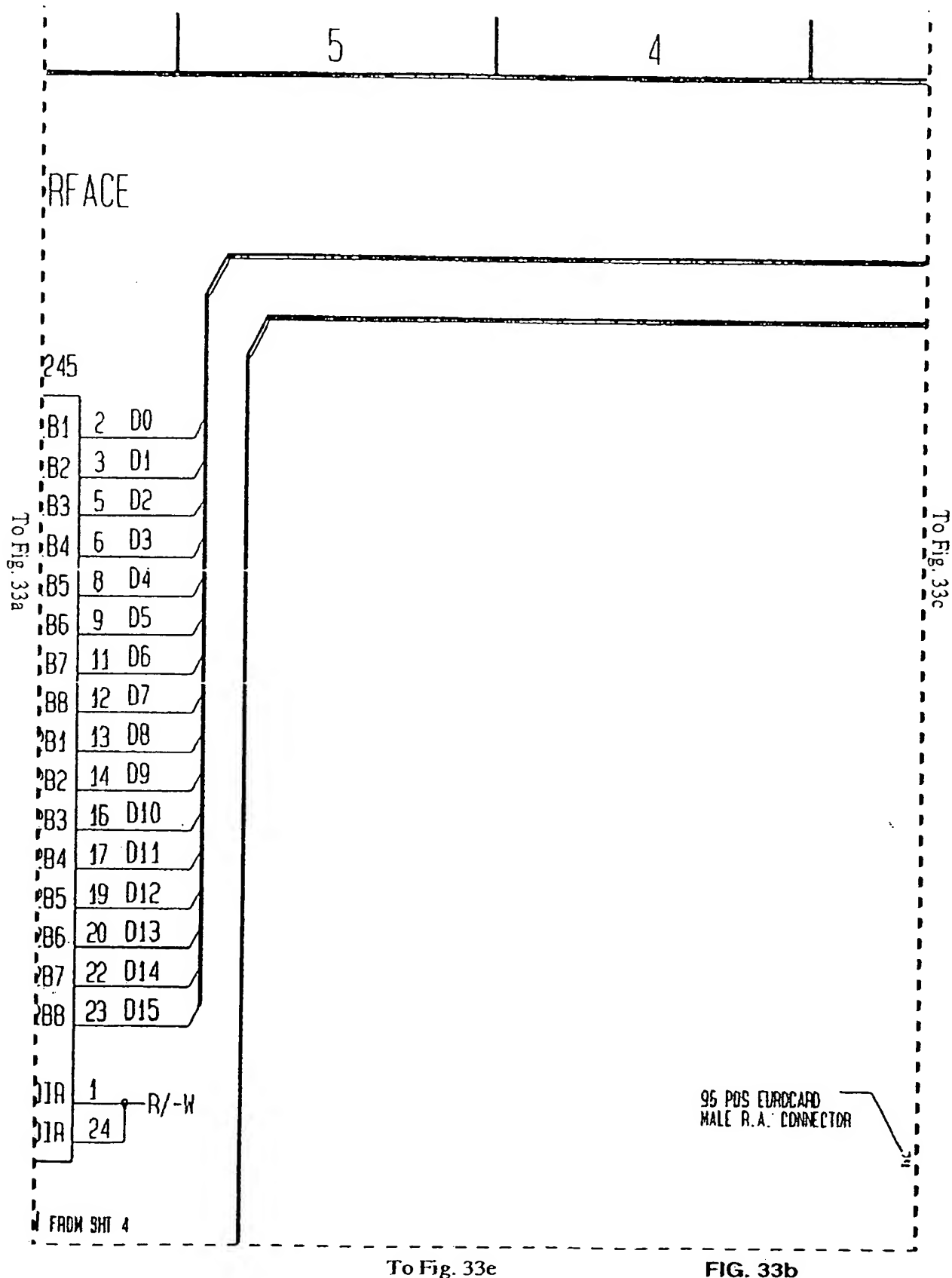
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FIG. 32i

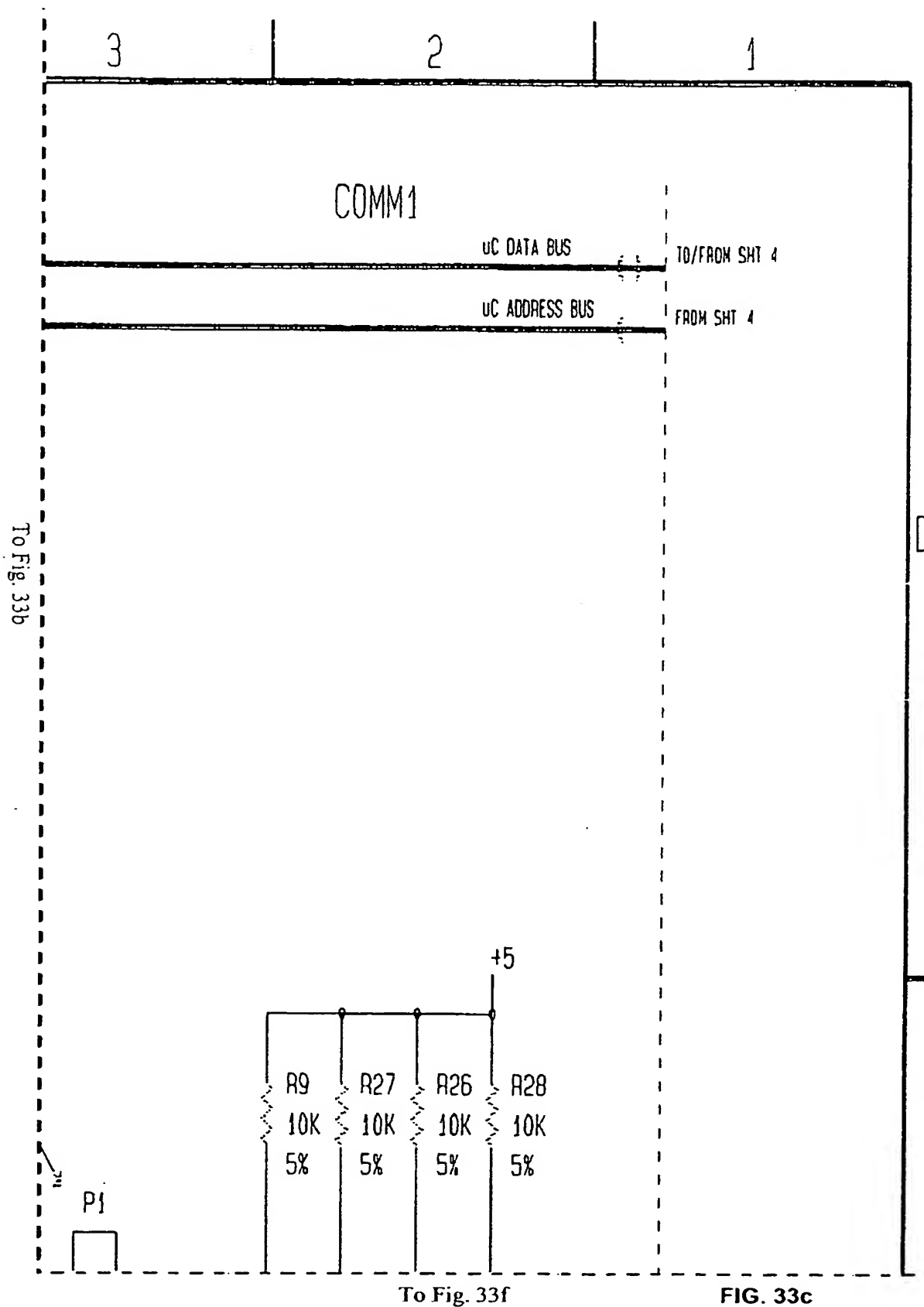
82 06 207



83 26 207



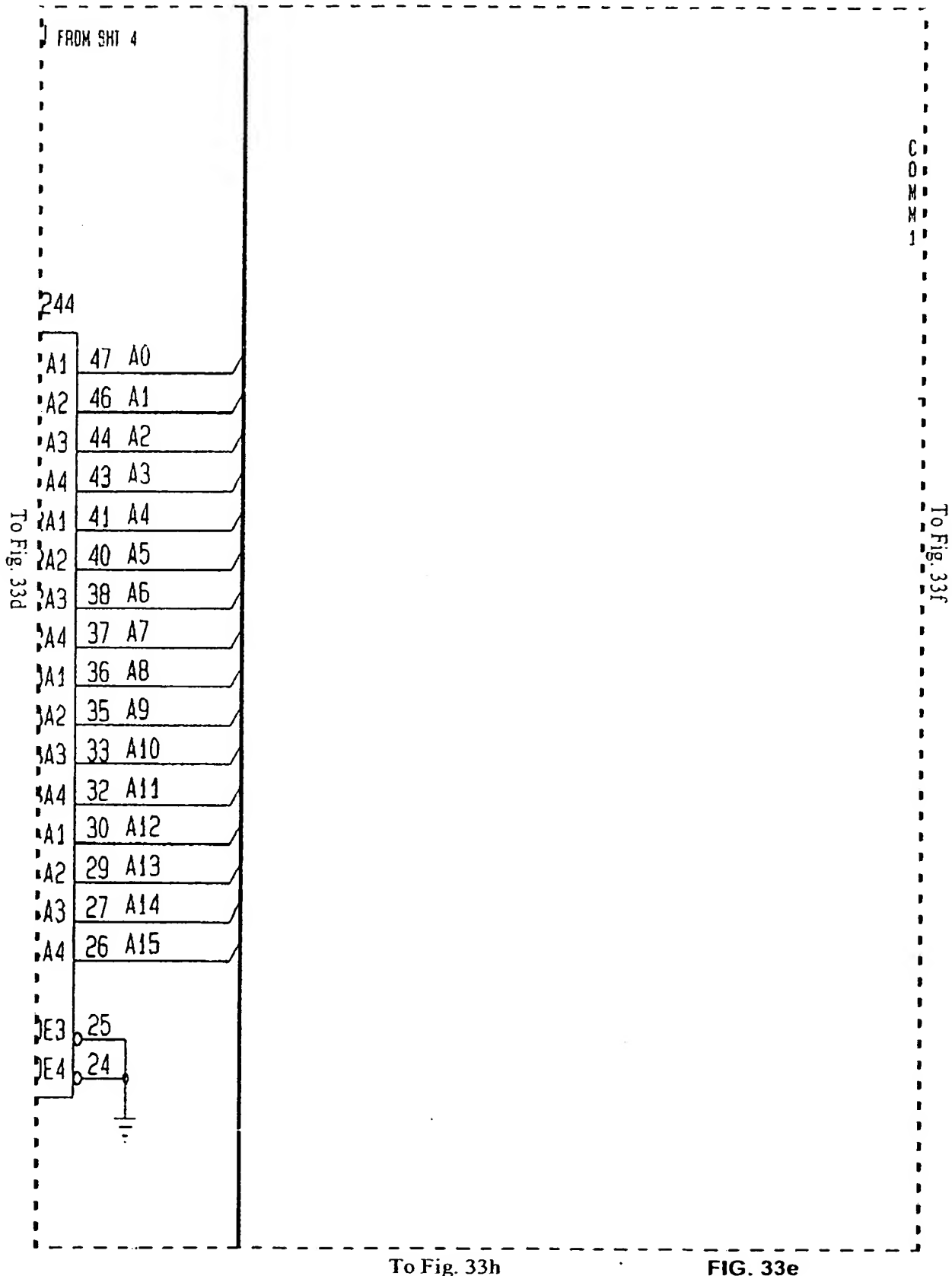
84 06 207







To Fig. 33b



To Fig. 33h

FIG. 33e

To Fig. 33c

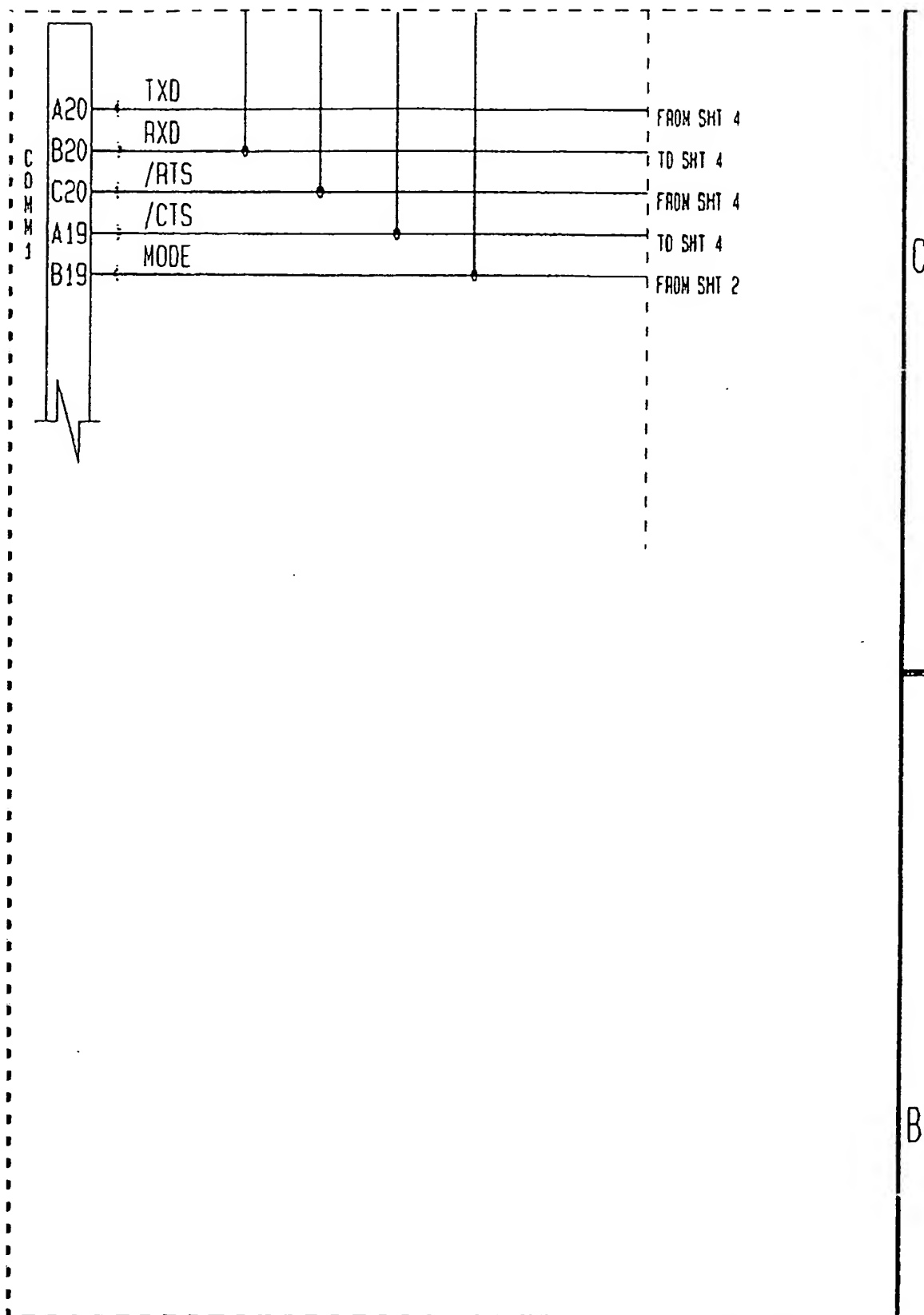
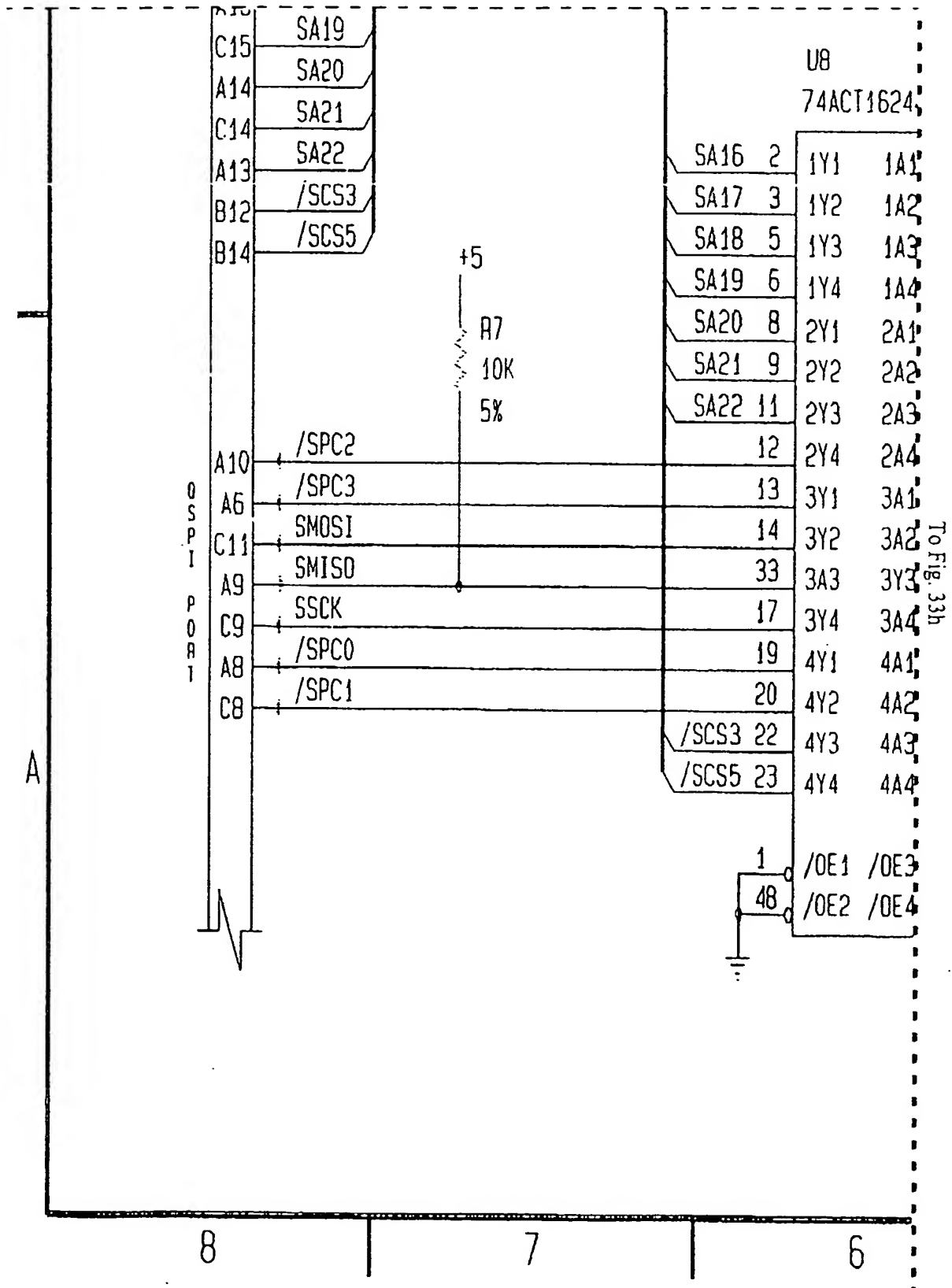


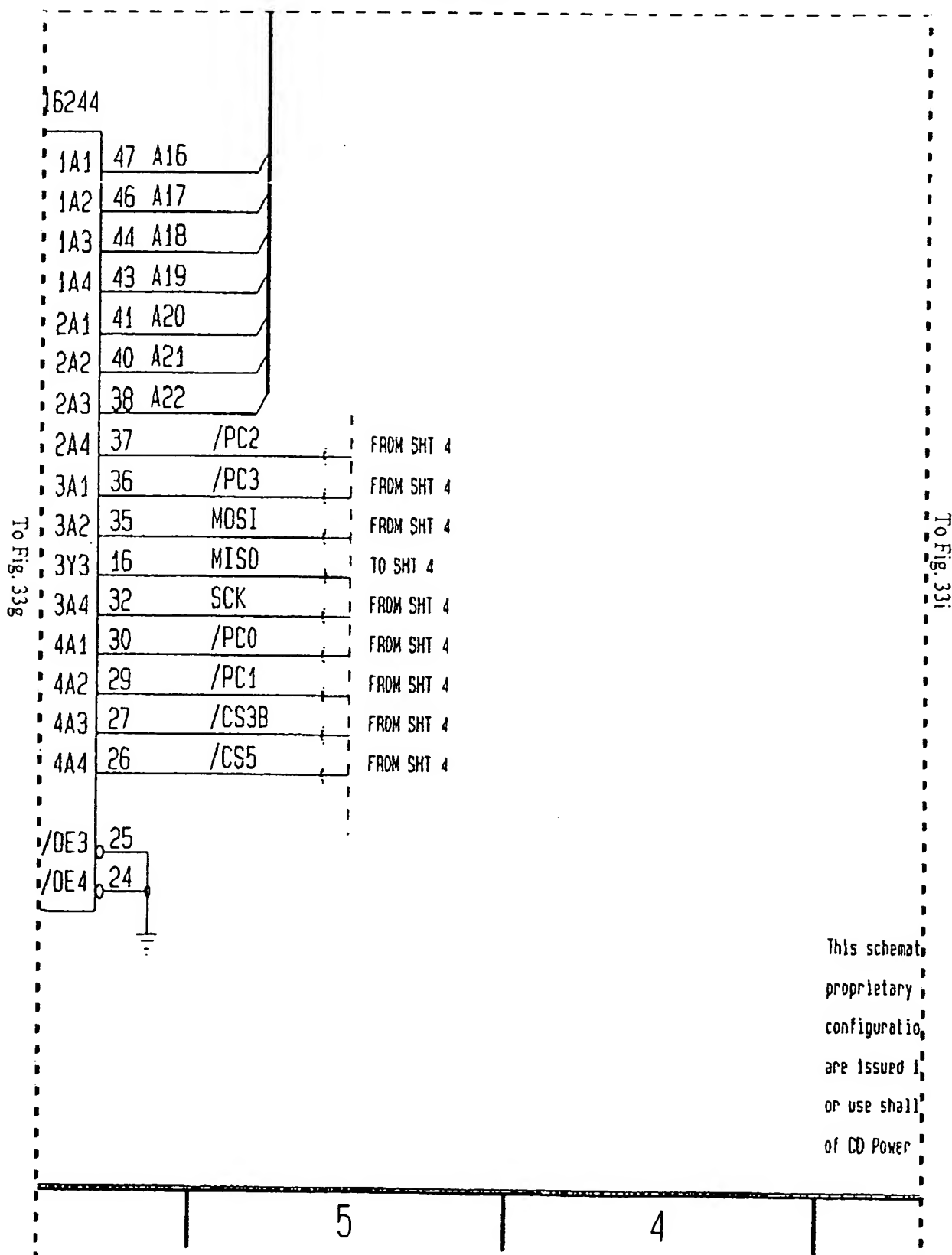
FIG. 33f

§ 8 J 07

To Fig. 33d



To Fig. 33c




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FIG. 33h

To Fig. 33f

To Fig. 33h

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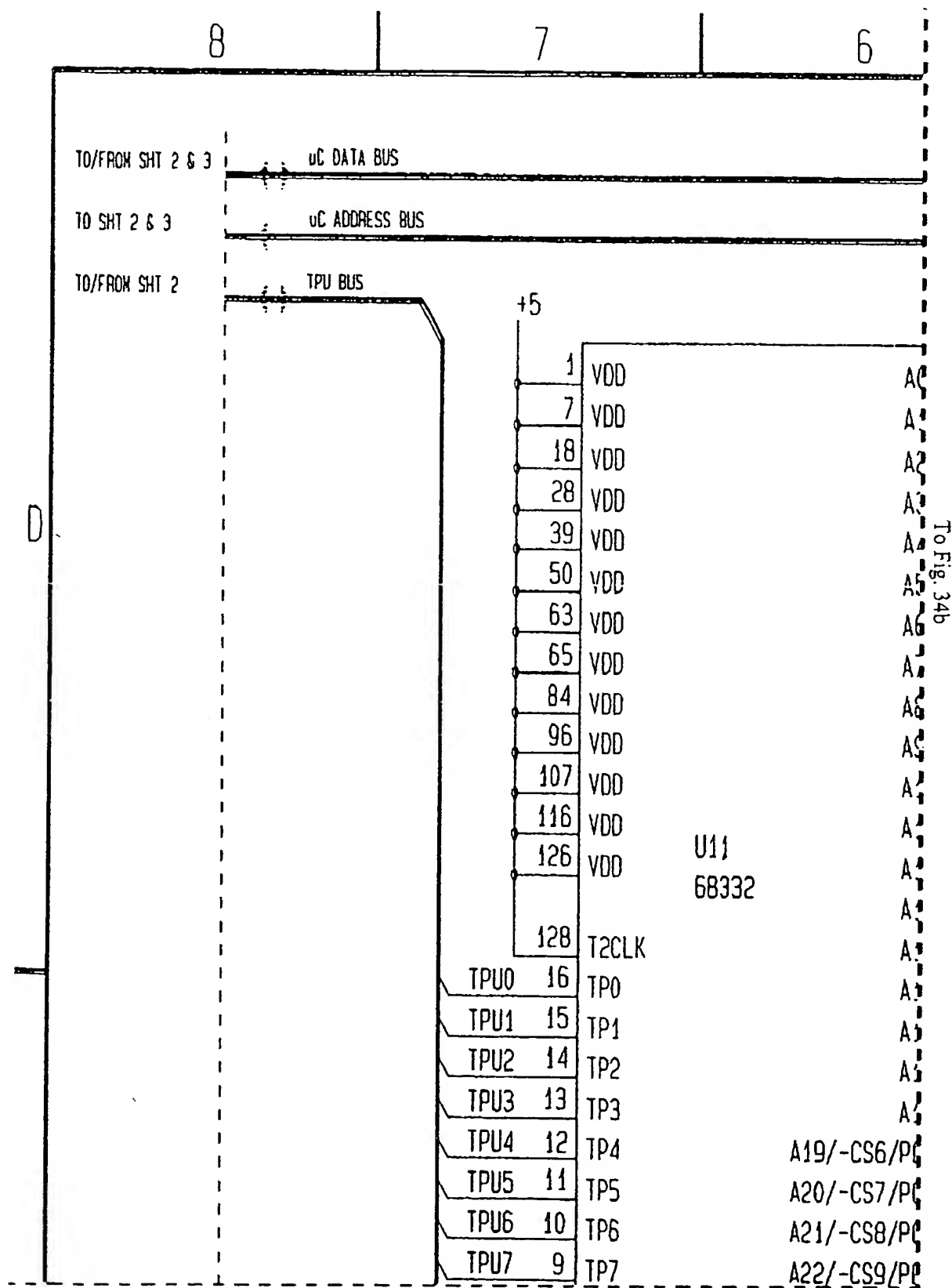
3

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1

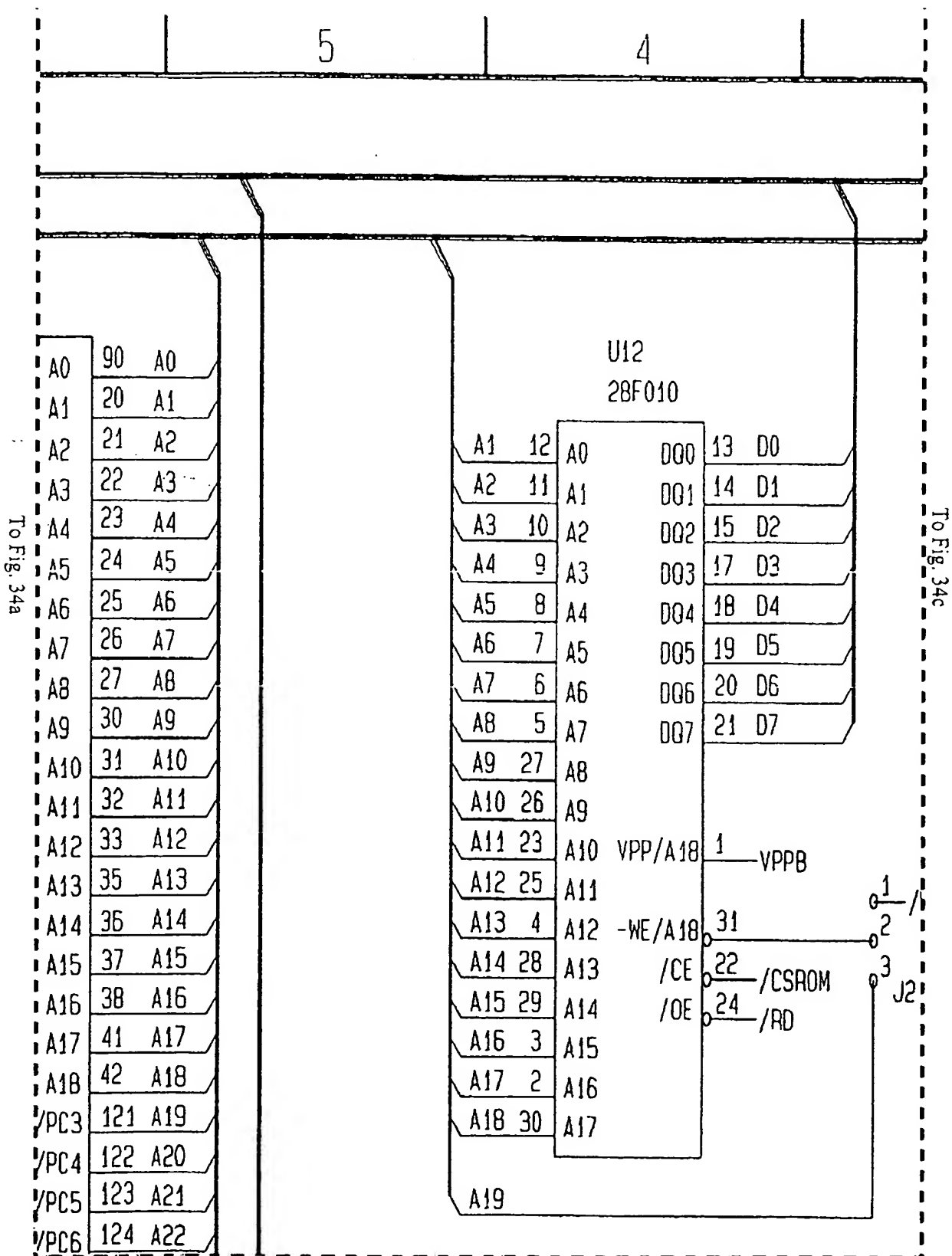
FIG. 33i

91 06 207



To Fig. 34d

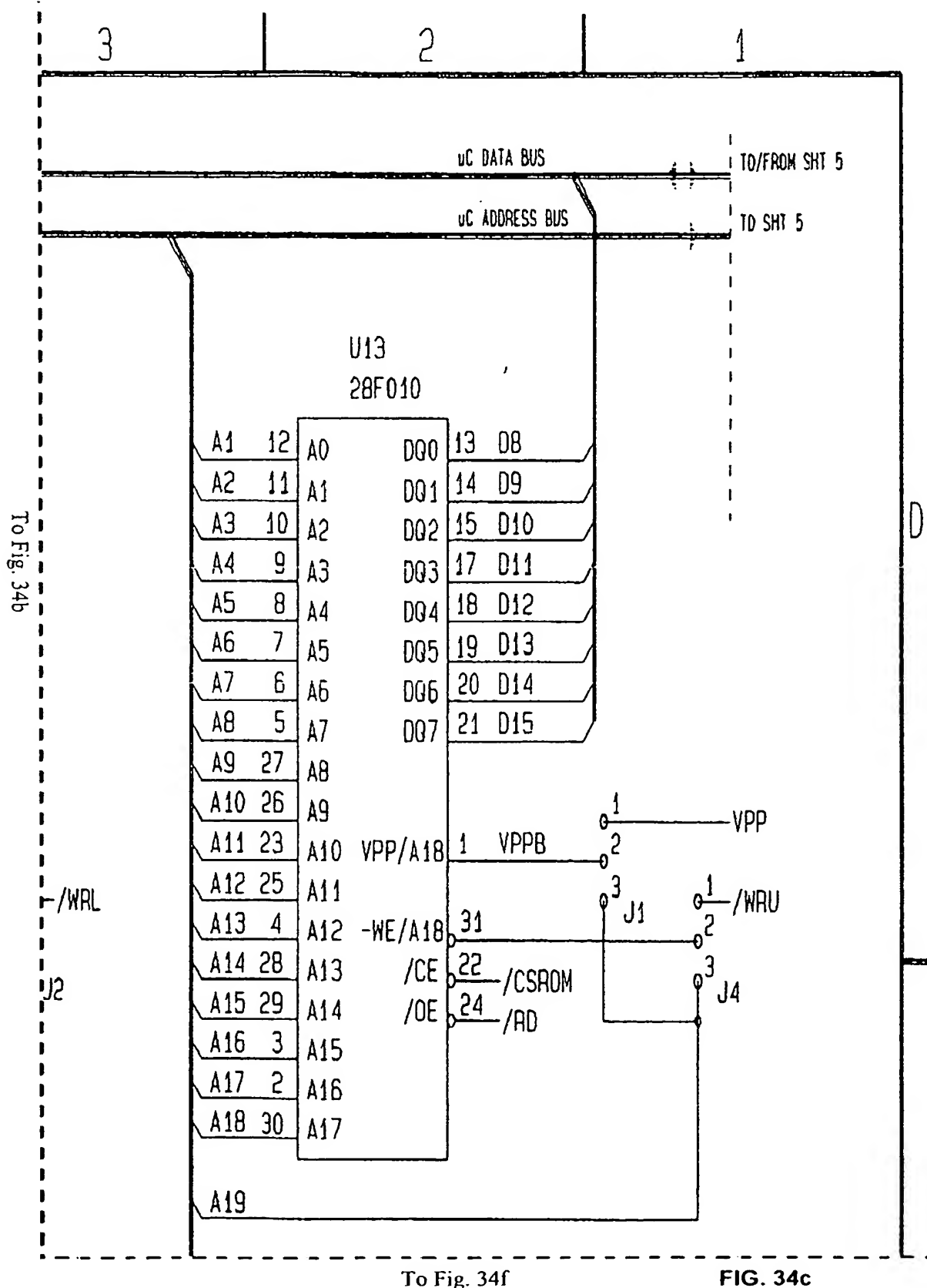
FIG. 34a



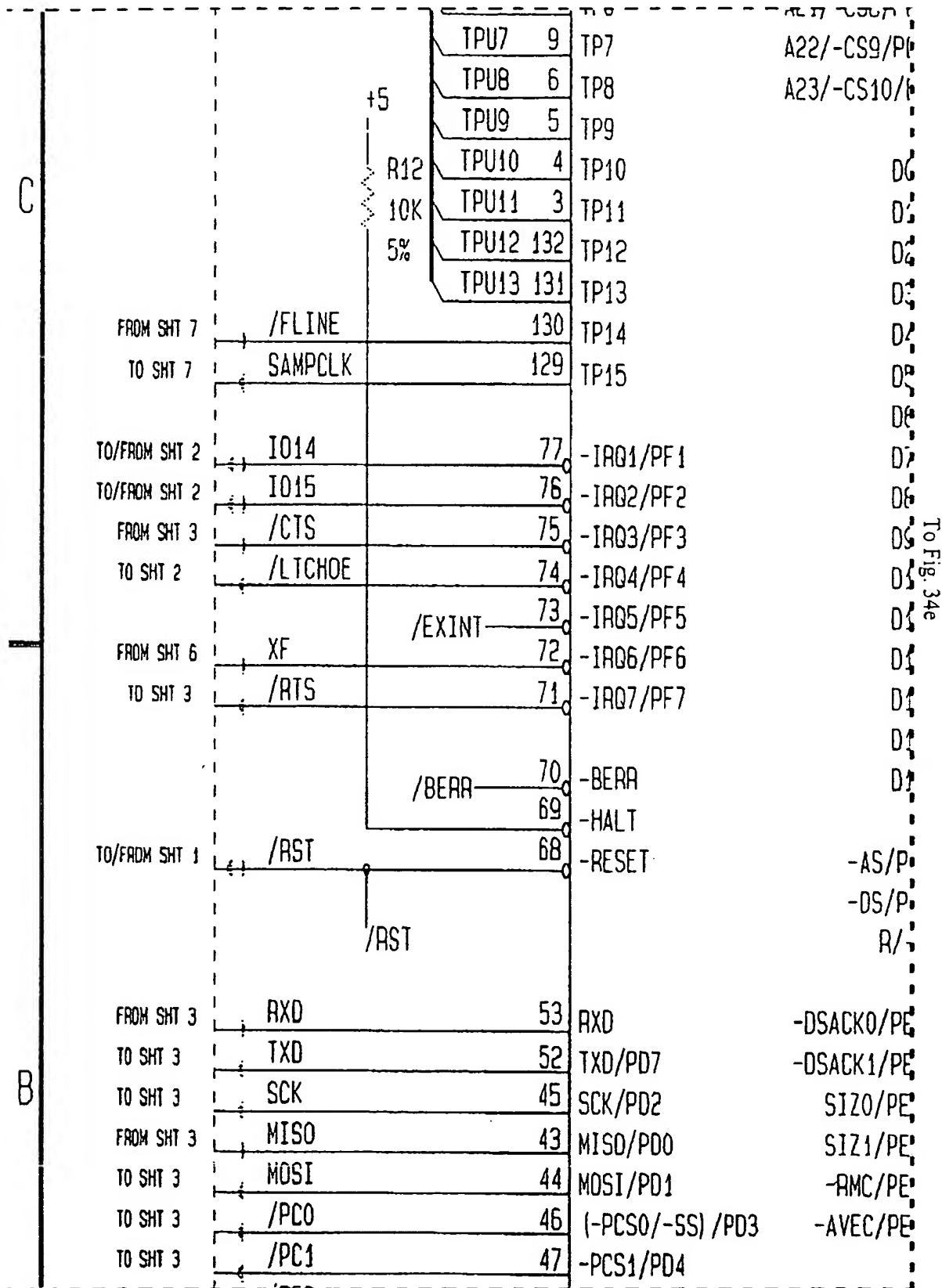
To Fig. 34e

FIG. 34b





To Fig. 34a

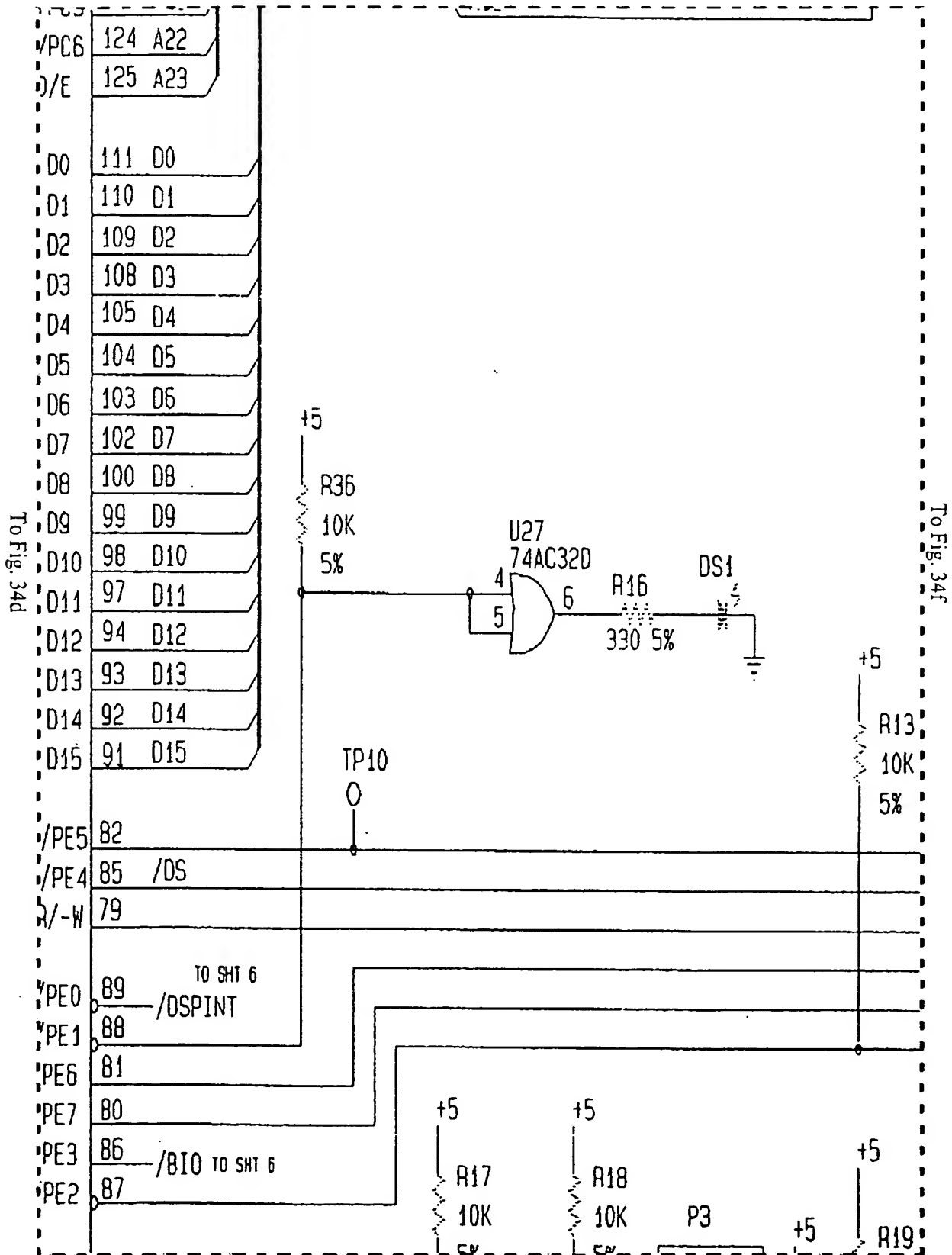


To Fig. 34g

FIG. 34d

45 of 267

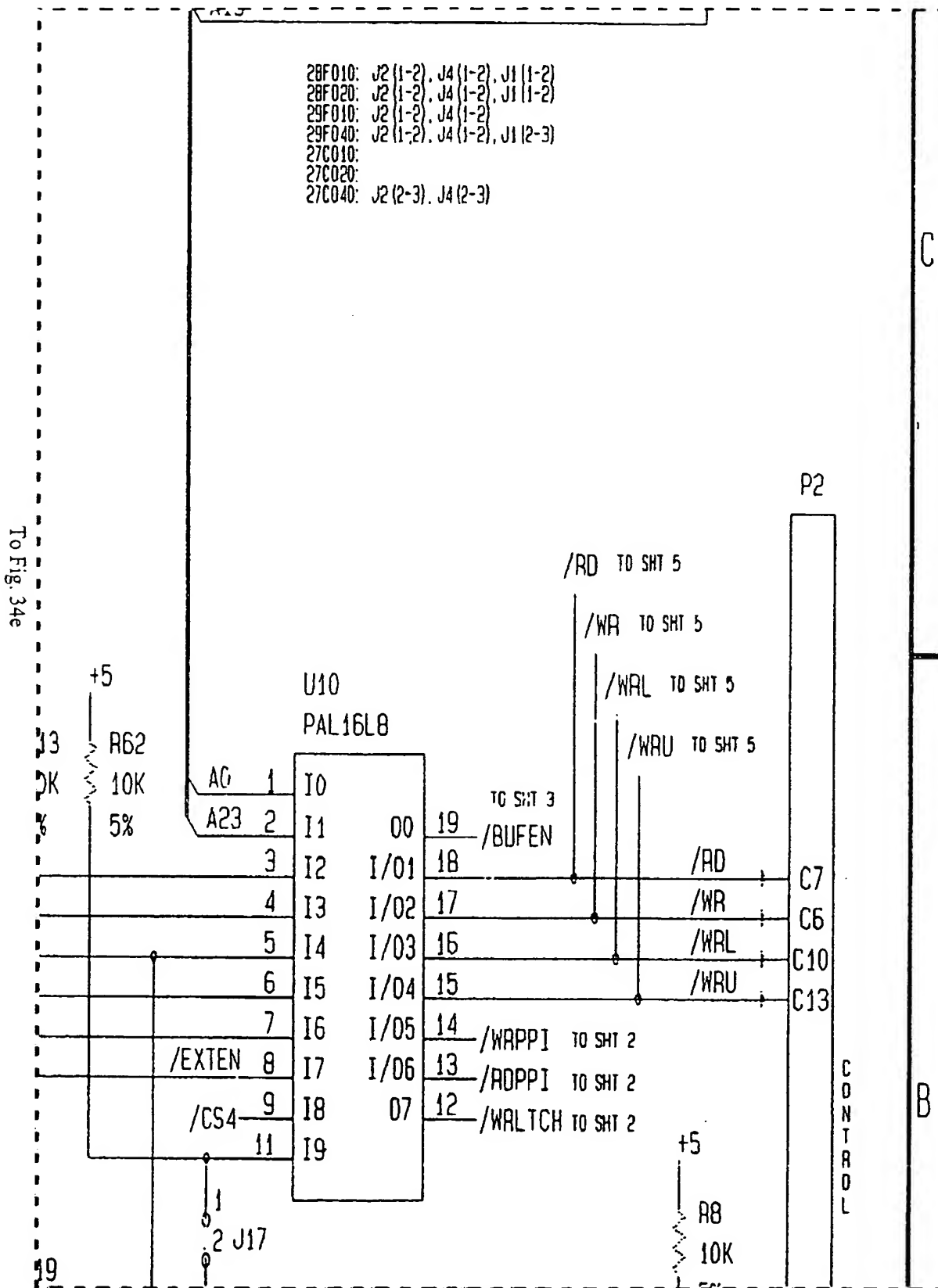
To Fig. 34b



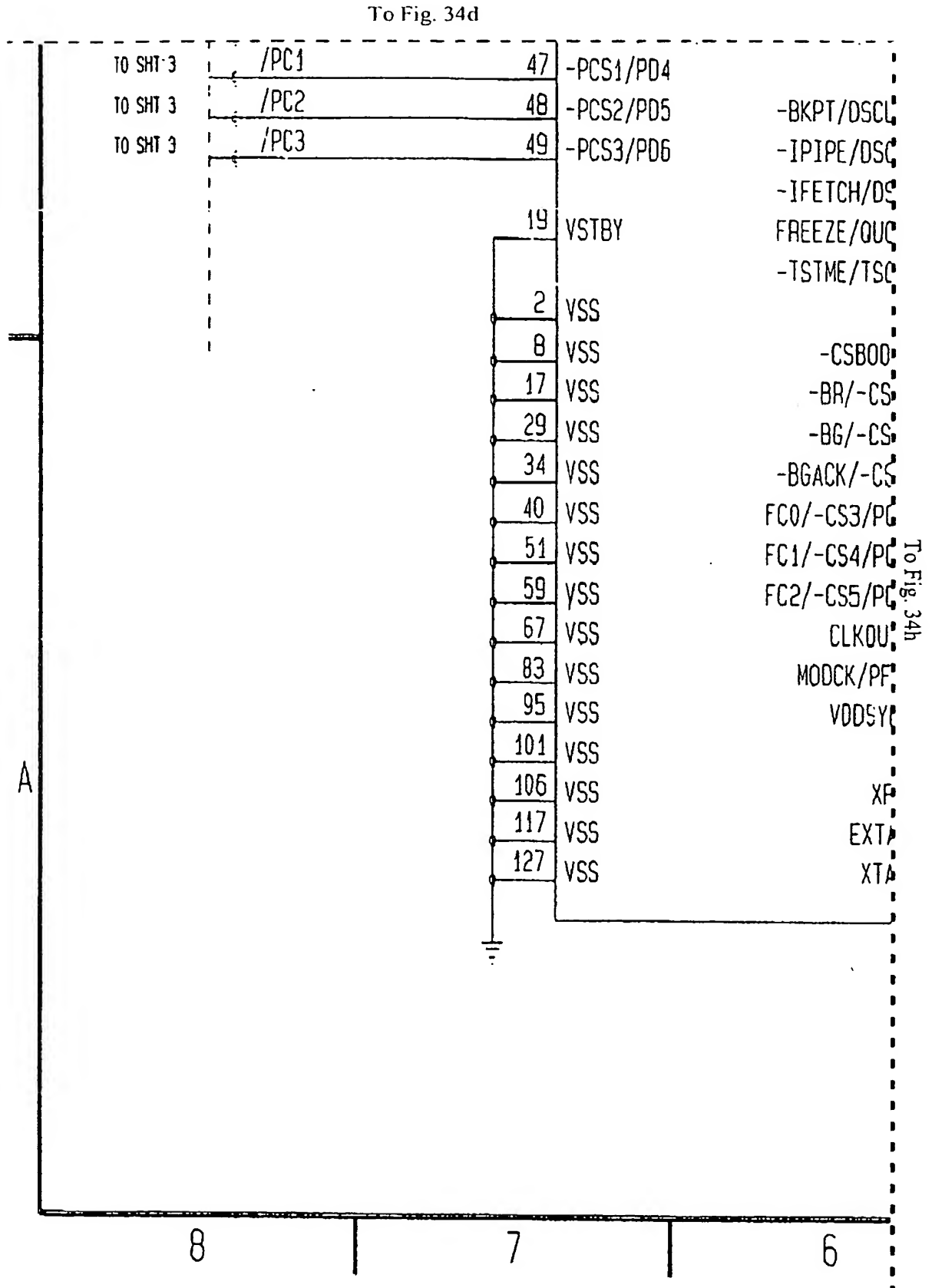
To Fig. 34h

FIG. 34e

To Fig. 34c



To Fig. 34i



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To Fig. 34e

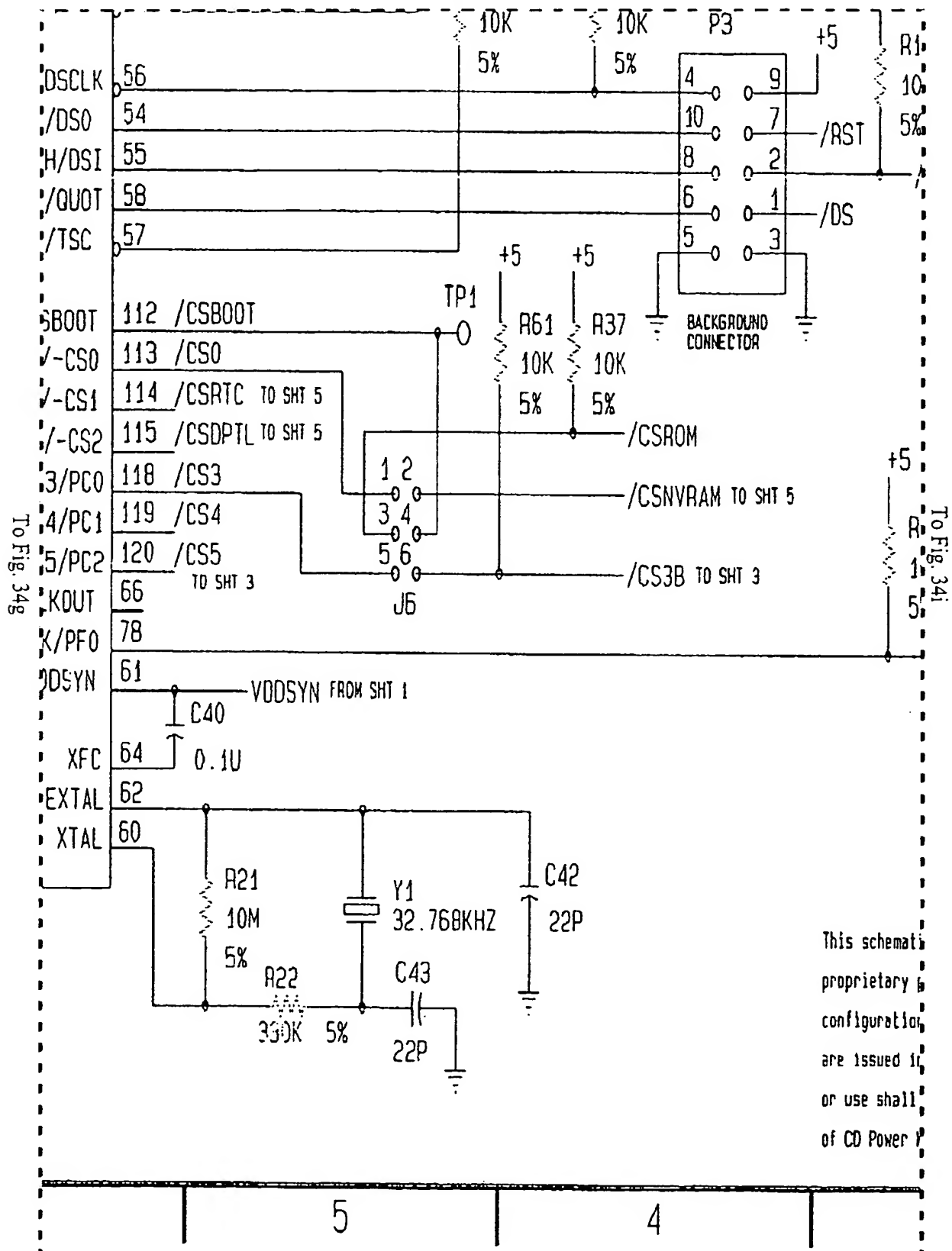
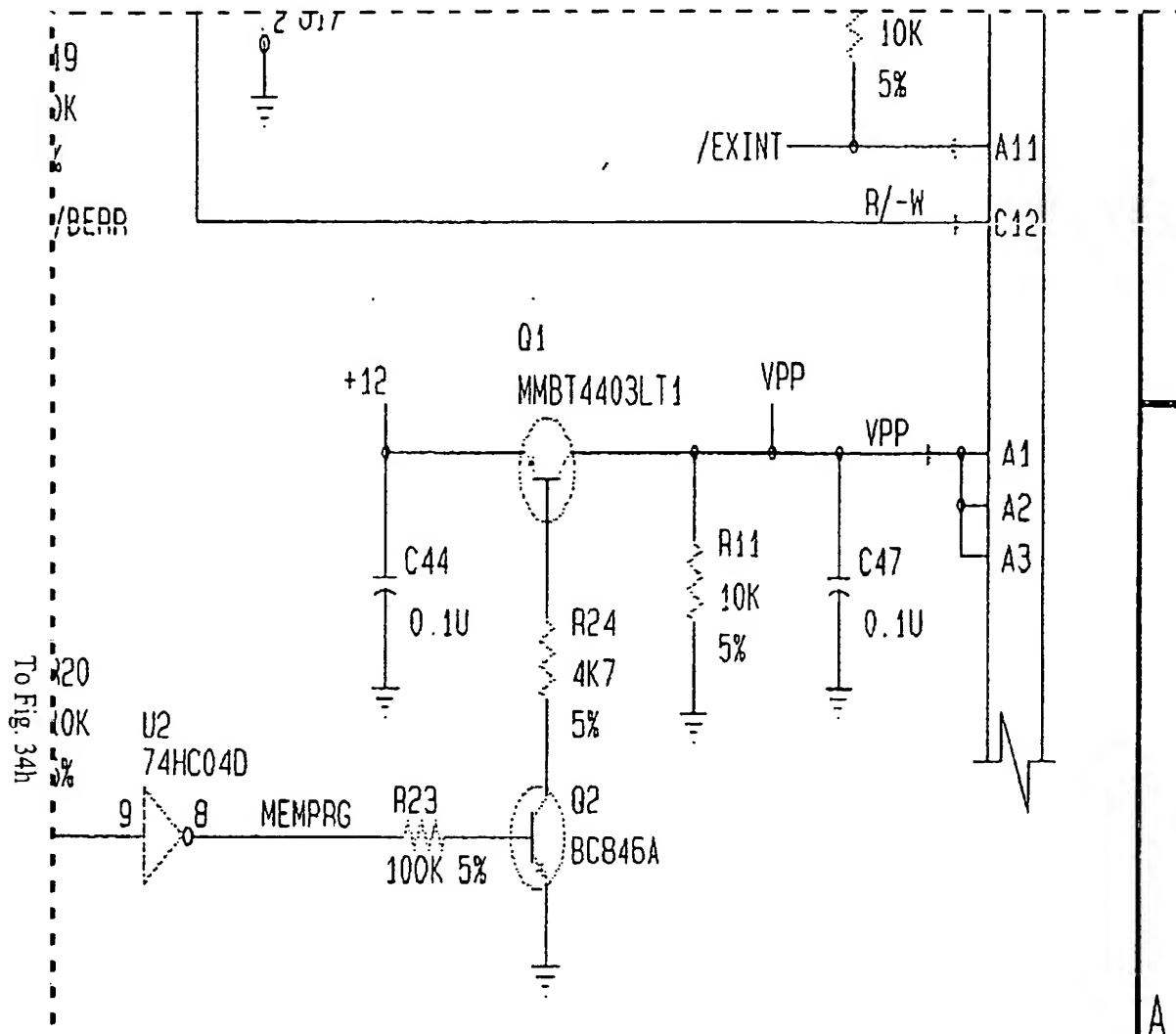


FIG. 34h

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To Fig. 34f



To Fig. 34h

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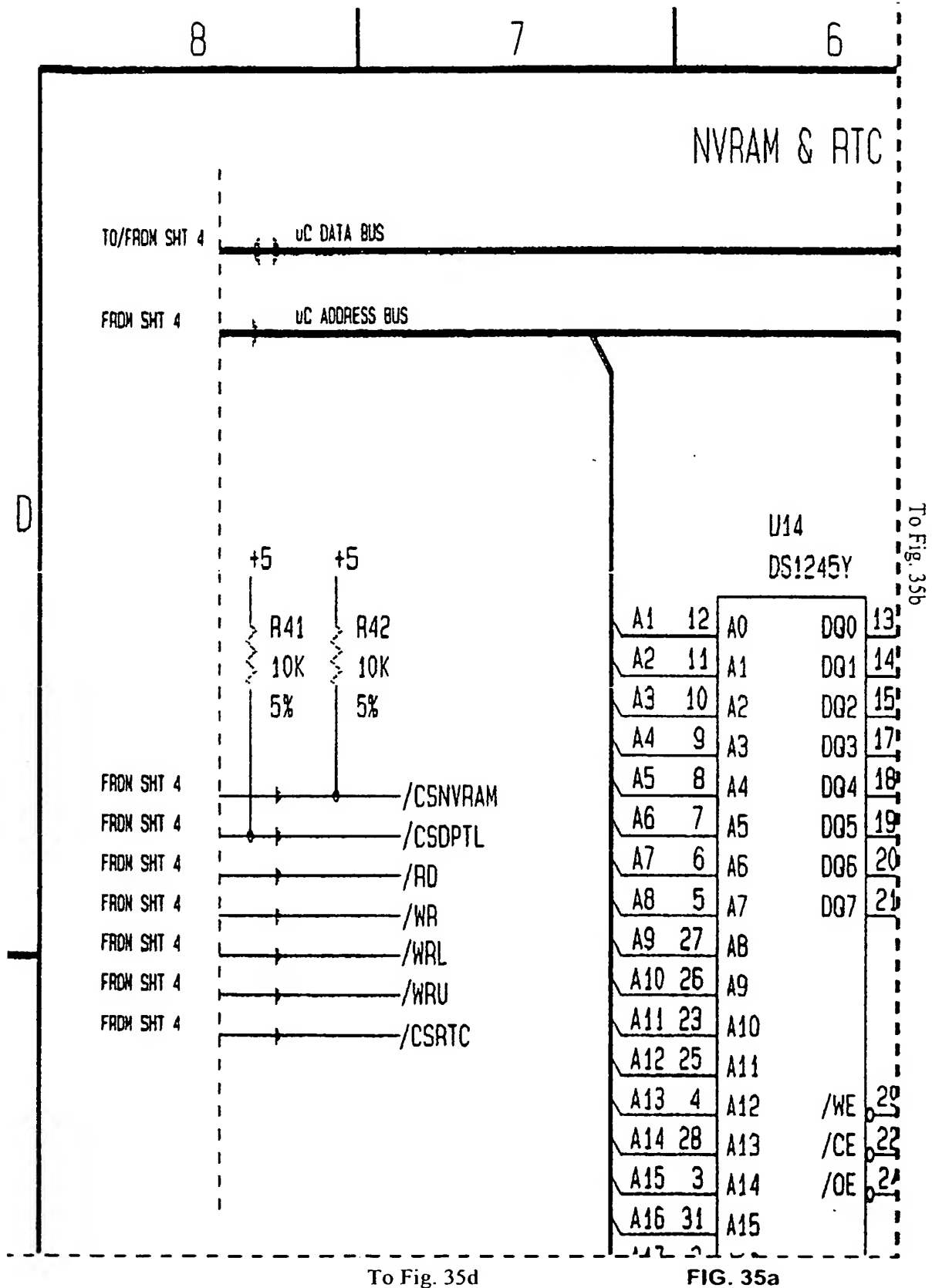
SHEET 4 OF 7

3

2

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FIG. 34i

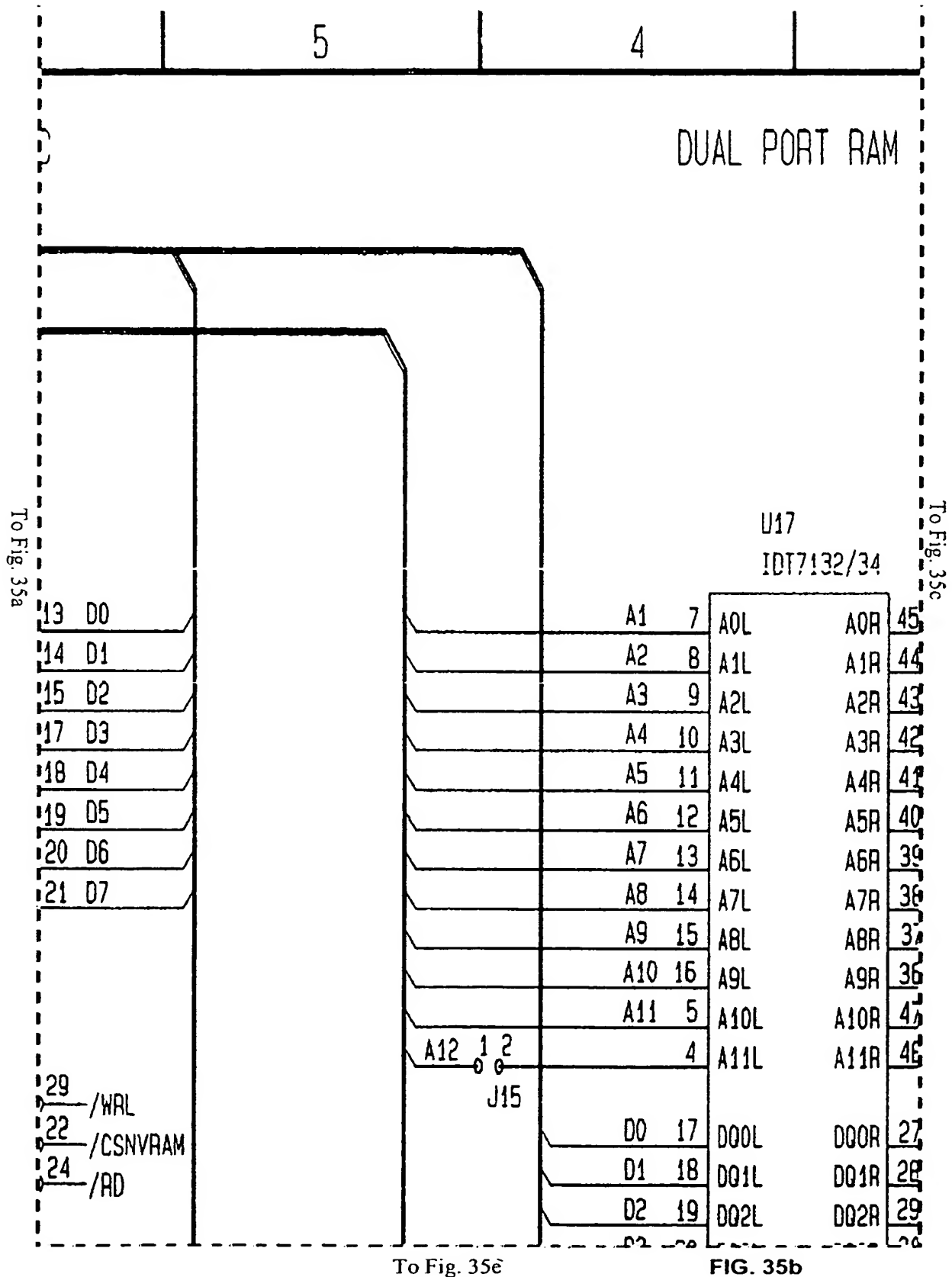


To Fig. 35d

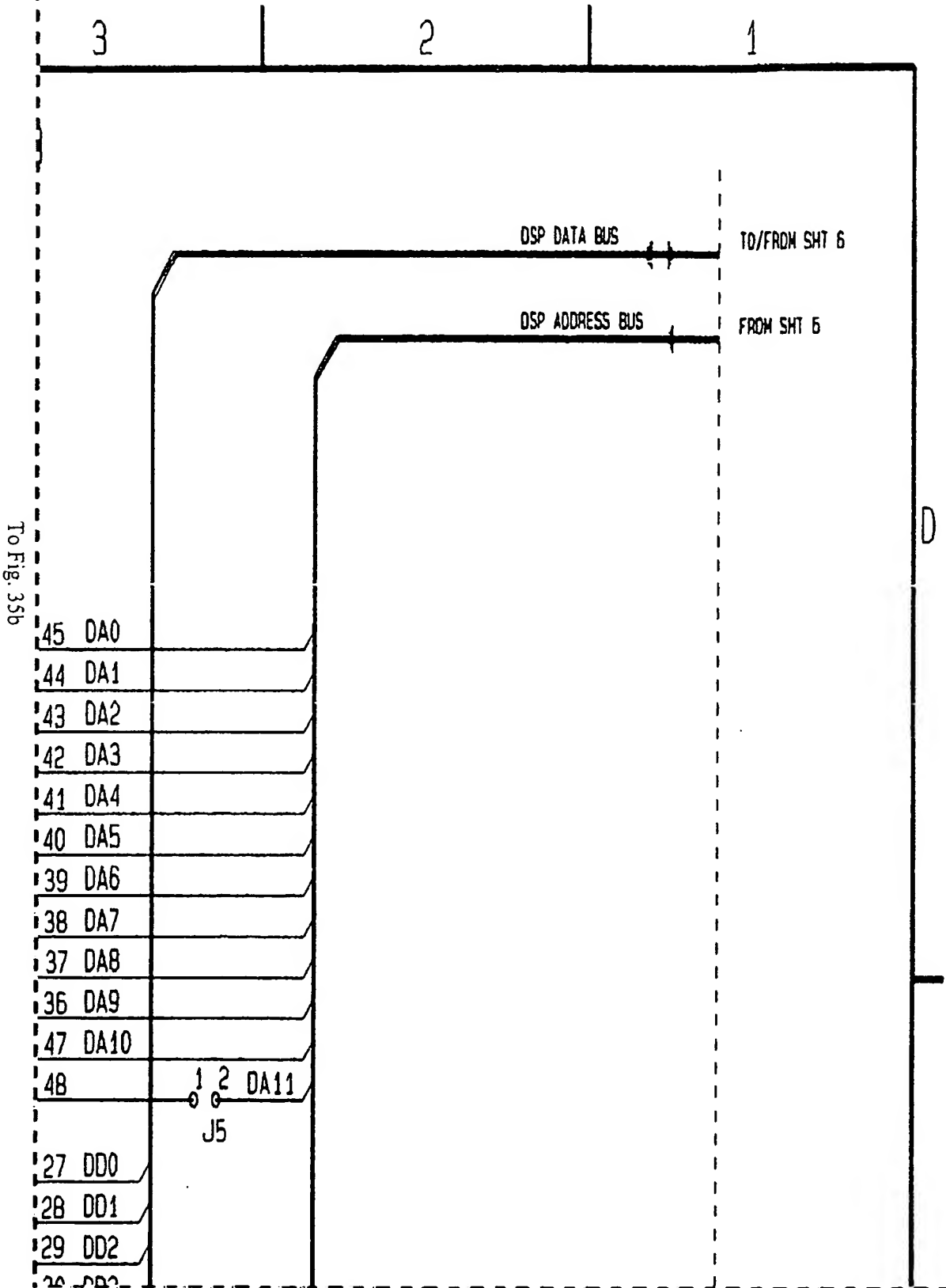
FIG. 35a



101 8 207



102 8207

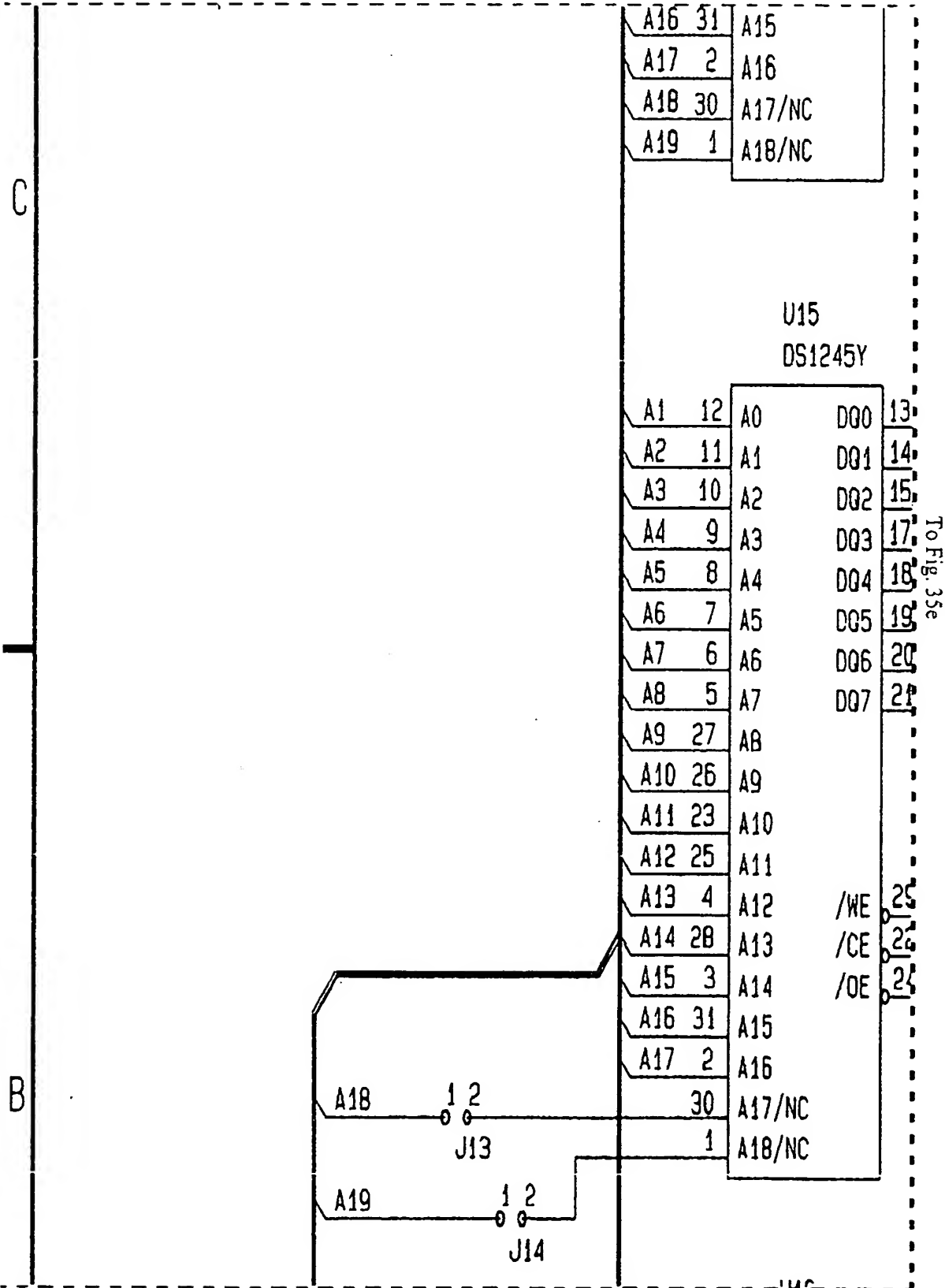


To Fig. 35f

FIG. 35c

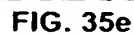
103 86 207

To Fig. 35a

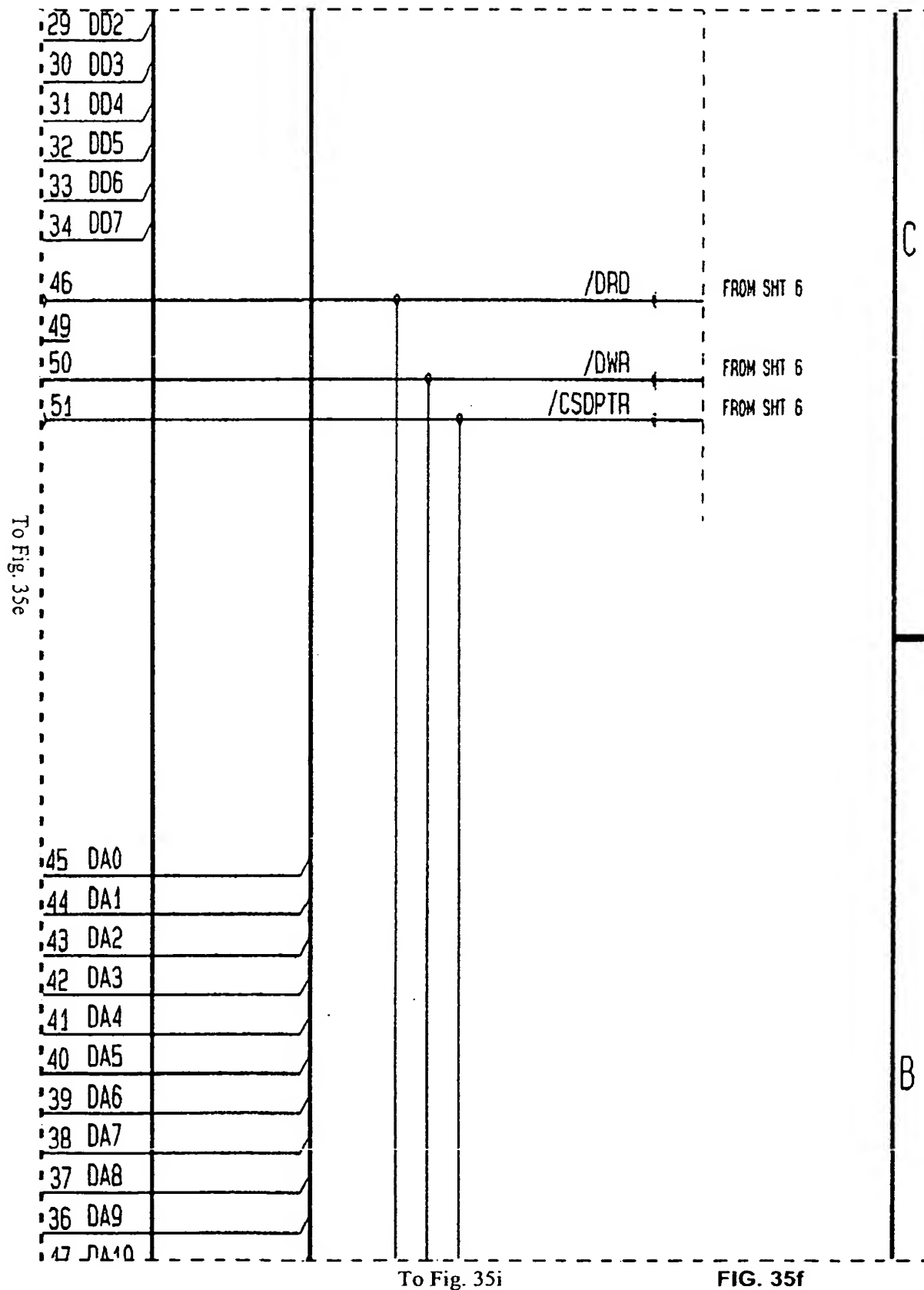


To Fig. 35g

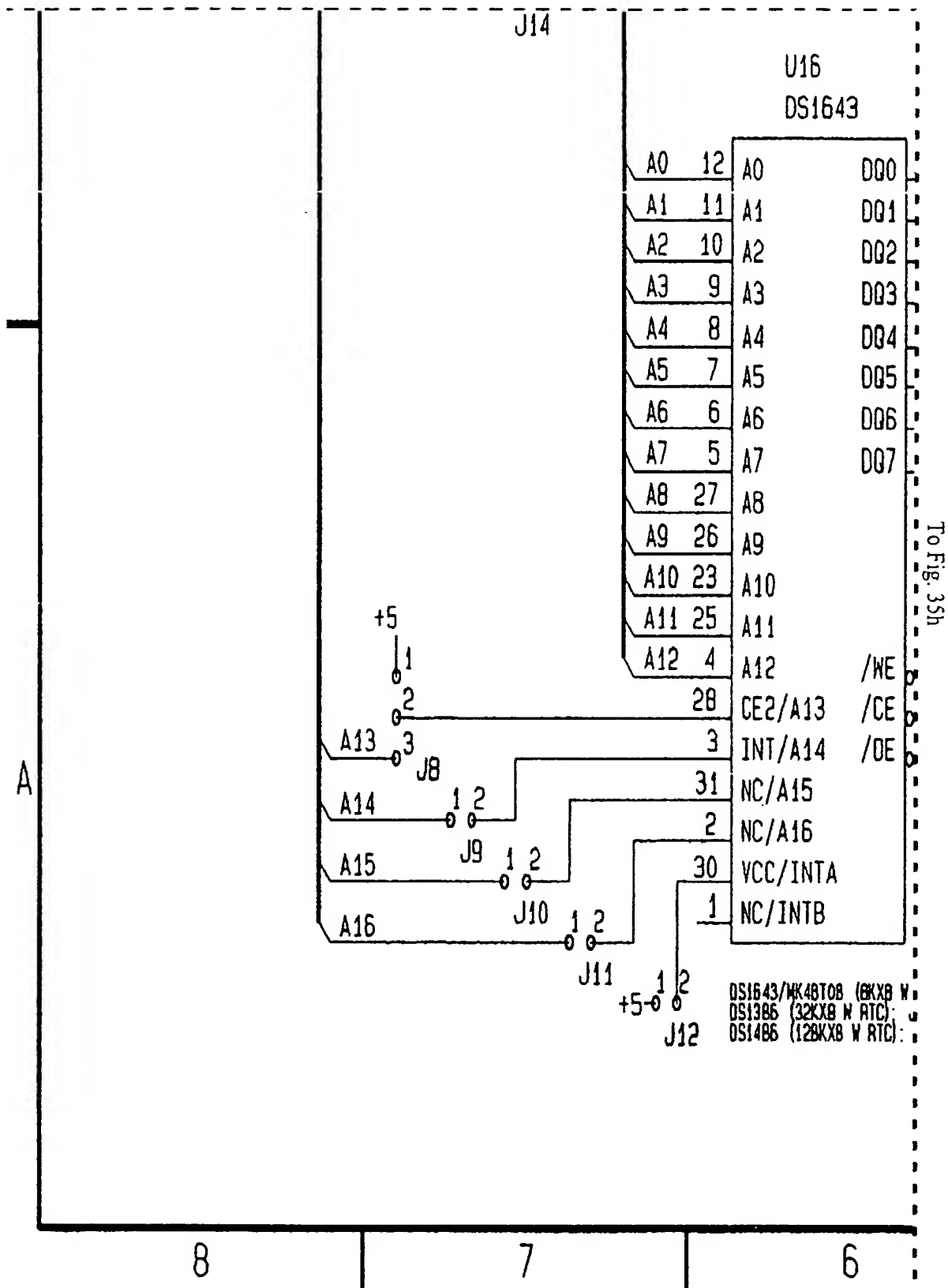
FIG. 35d



To Fig. 35c



To Fig. 35d



107 06 207

To Fig. 35e

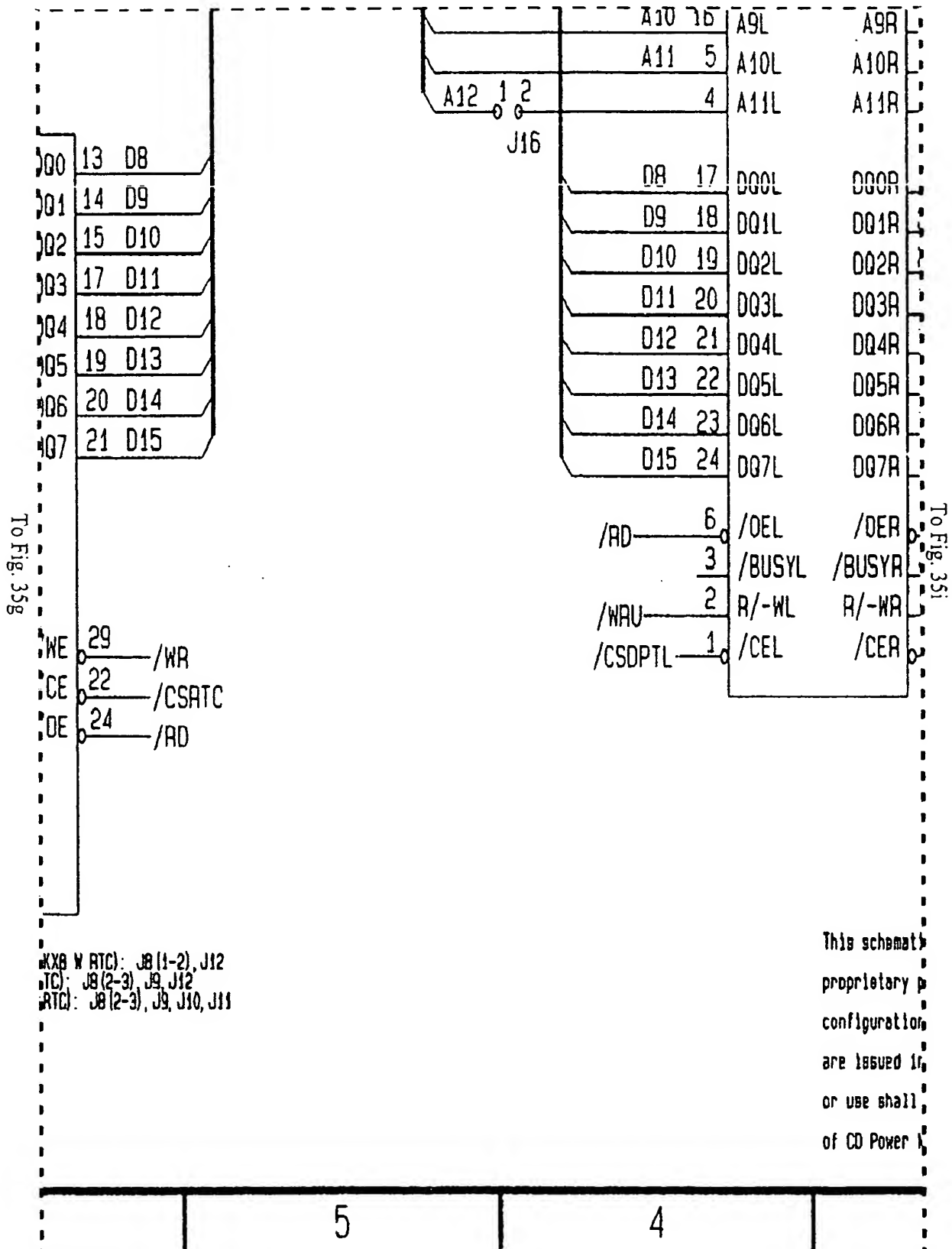
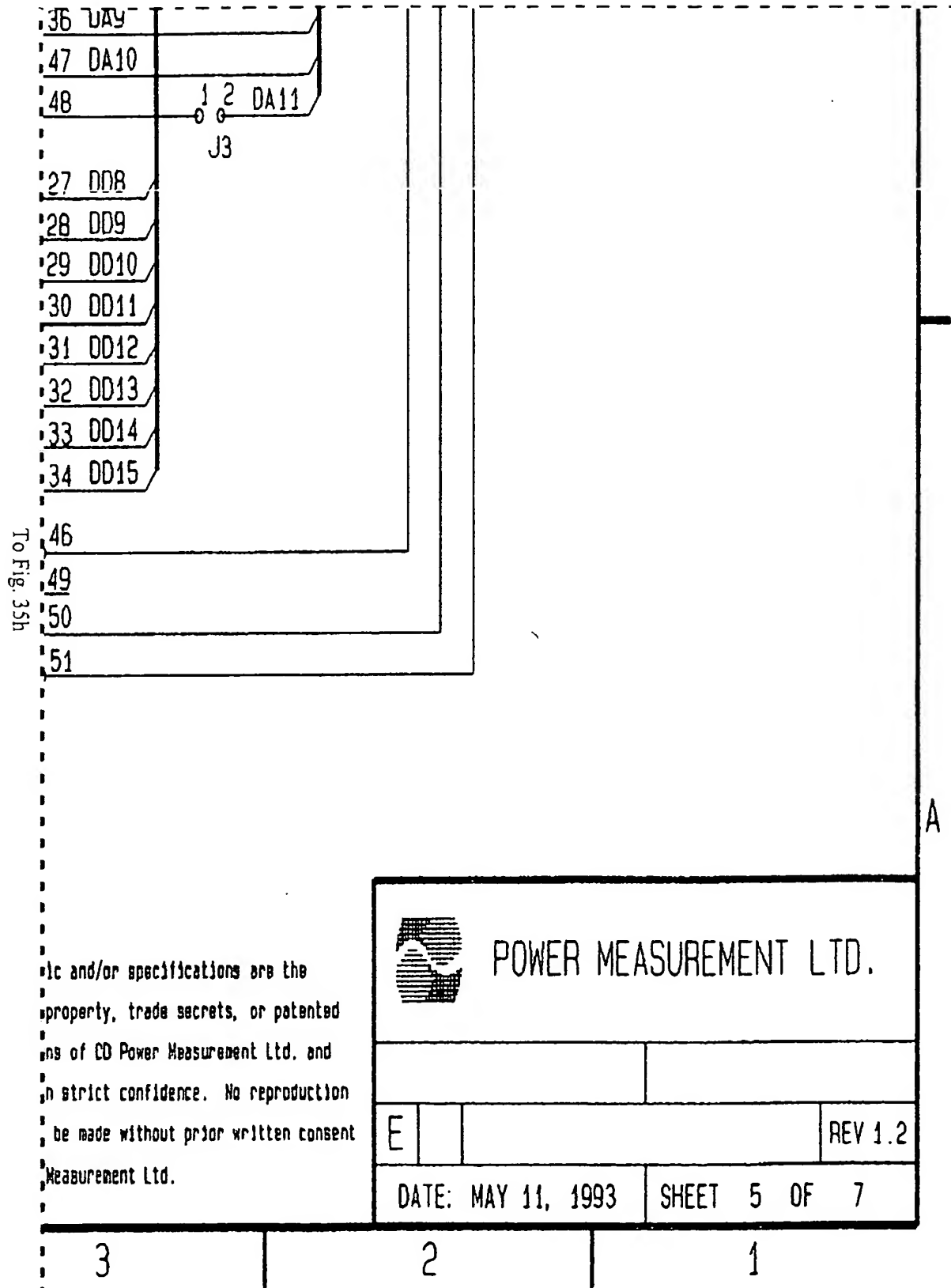


FIG. 35h

108 9207

To Fig. 35f

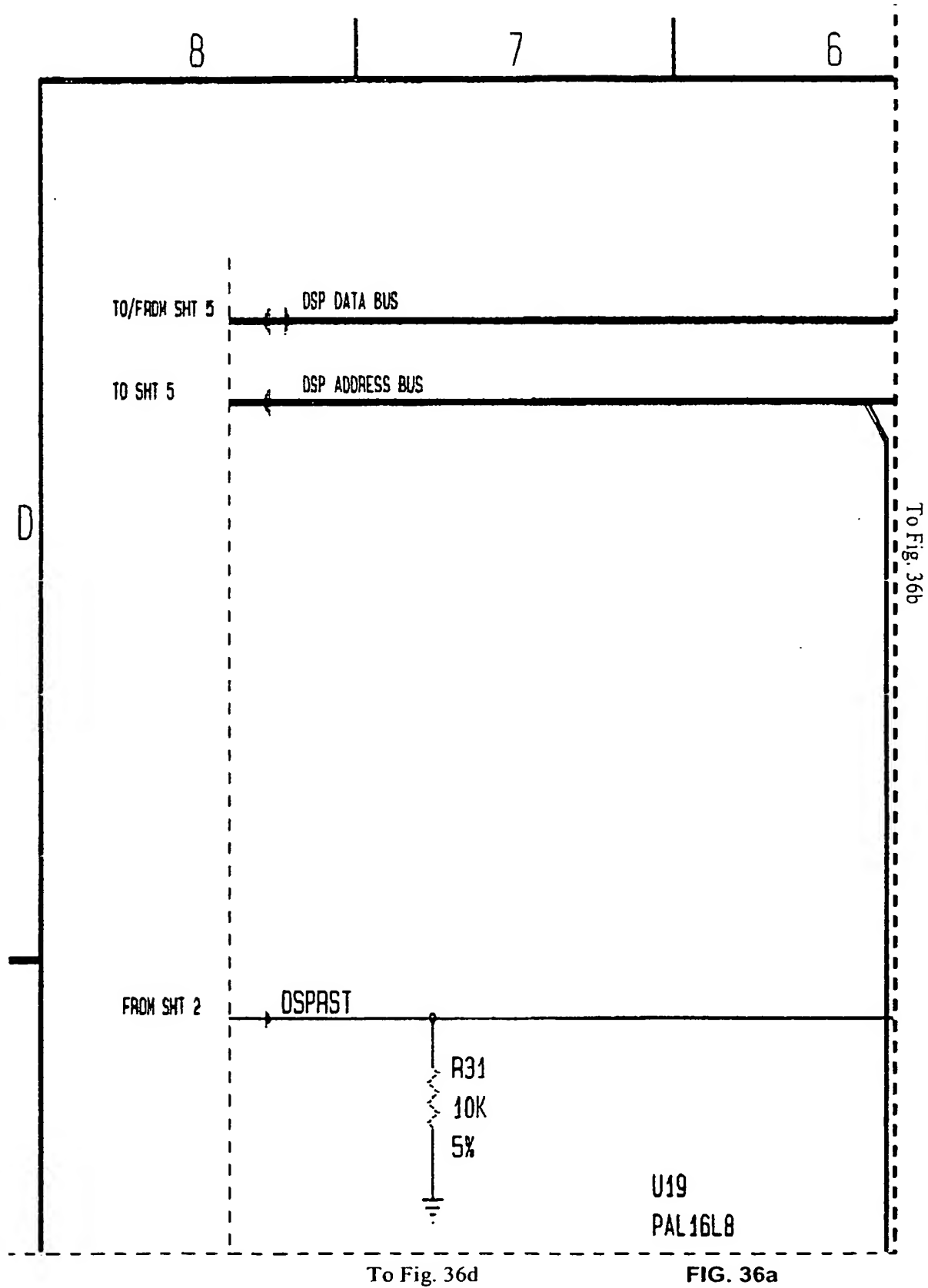


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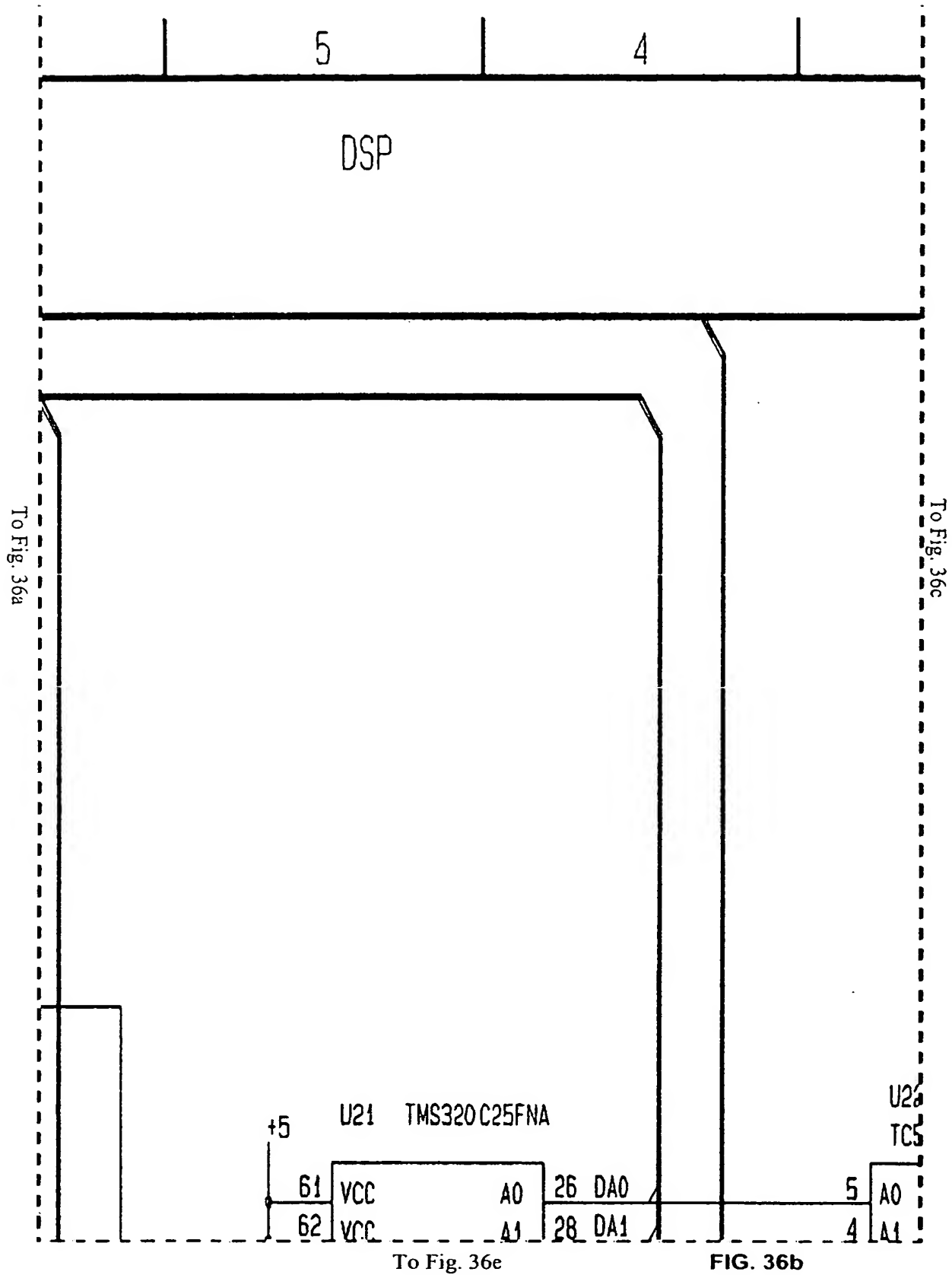
FIG. 35i

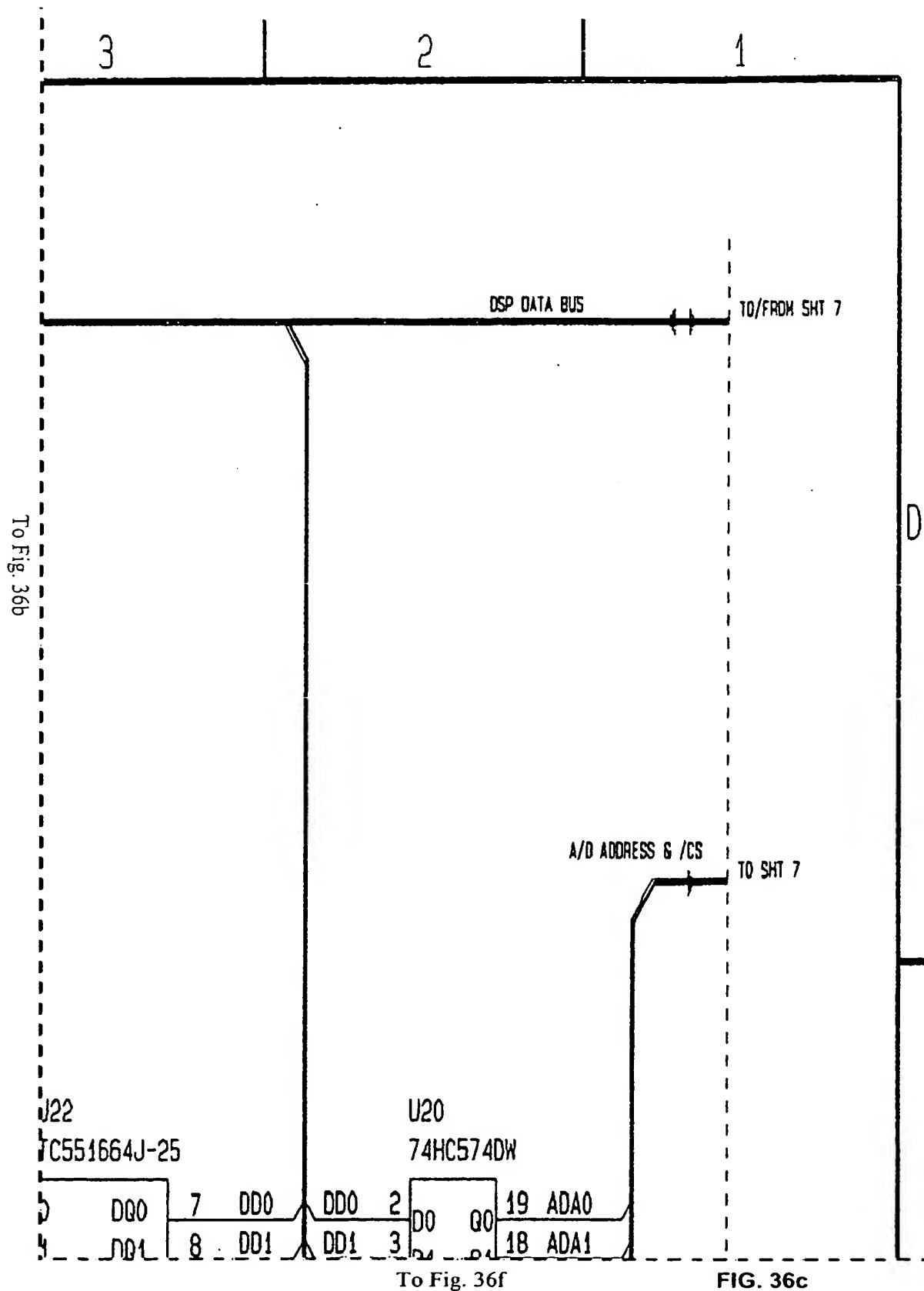


109 B 207



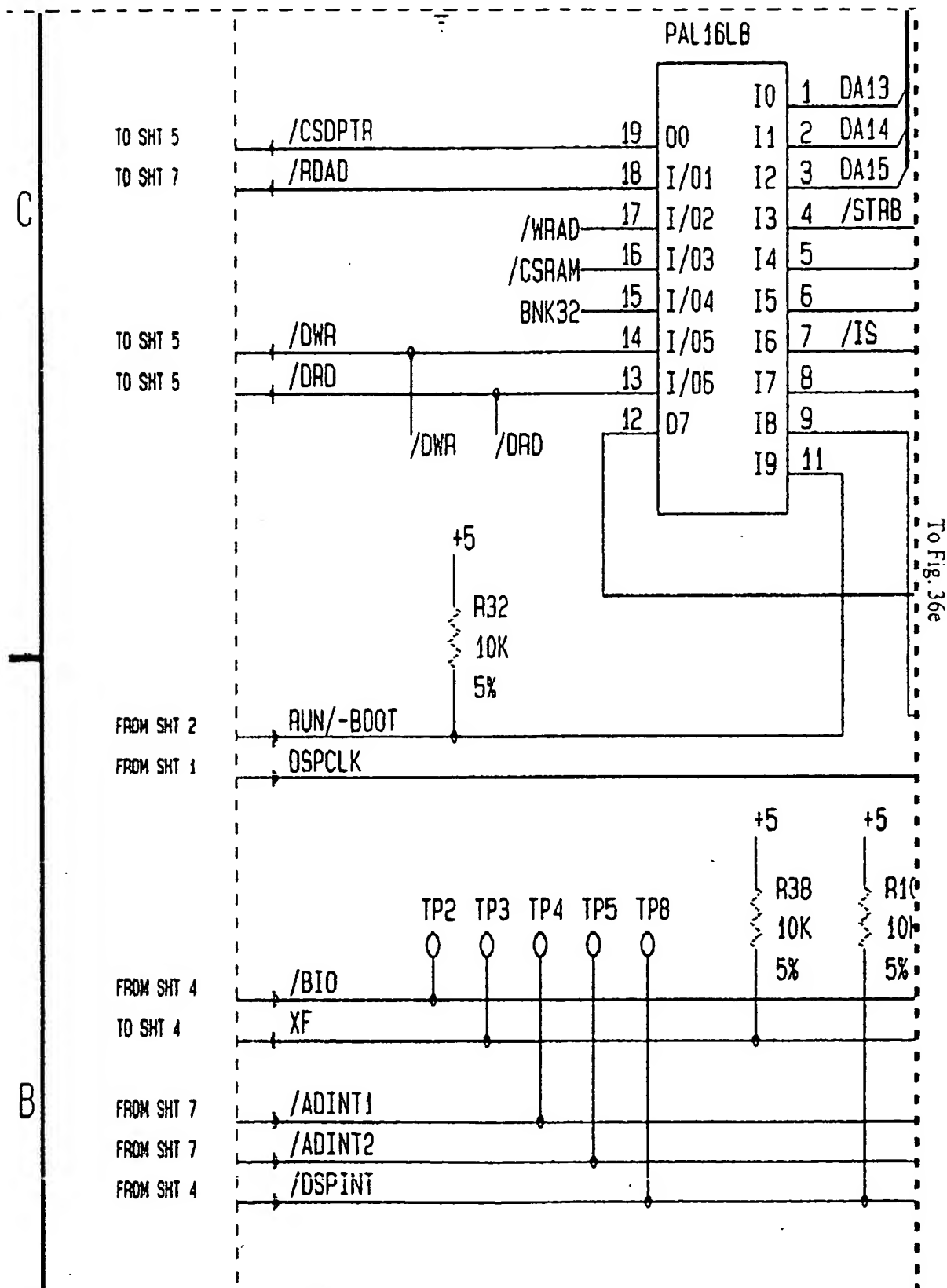
110 86 207





112 8 2-07

To Fig. 36a

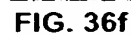


To Fig. 36g

FIG. 36d

Pin	Signal	Pin	Signal	Pin	Signal
62	VCC	A1	28 DA1	4	A1
23	VCC	A2	29 DA2	3	A2
35	VCC	A3	30 DA3	2	A3
		A4	31 DA4	1	A4
49	/STRB	A5	32 DA5	44	A5
48	R/-W	A6	33 DA6	43	A6
47	/PS	A7	34 DA7	42	A7
46	/IS	A8	36 DA8	27	A8
45	/DS	A9	37 DA9	26	A9
		A10	38 DA10	25	A10
65	/RS	A11	39 DA11	24	A11
67	/HOLD	A12	40 DA12	21	A12
55	/HOLDA	A13	41 DA13	20	A13
66	READY	A14	42 DA14	19	A14
50	/BR	A15	43 DA15	18	A15
19	/SYNC			BNK32	
59	/MSC	D0	18 DD0	39	/LB
1	MP/-MC	D1	17 DD1	40	/UB
		D2	16 DD2		
58	CLKOUT 1	D3	15 DD3		
57	CLKOUT 2	D4	14 DD4		
52	X2/CLKIN	D5	13 DD5		
51	X1	D6	12 DD6		
68	/BIO	D7	11 DD7		
56	XF	D8	9 DD8		
		D9	8 DD9		
20	/INT0	D10	7 DD10		
21	/INT1	D11	6 DD11		
22	/INT2	D12	5 DD12		
60	/IACK	D13	4 DD13		
		D14	3 DD14		

**FIG. 36e**



115 08 207

To Fig. 36d

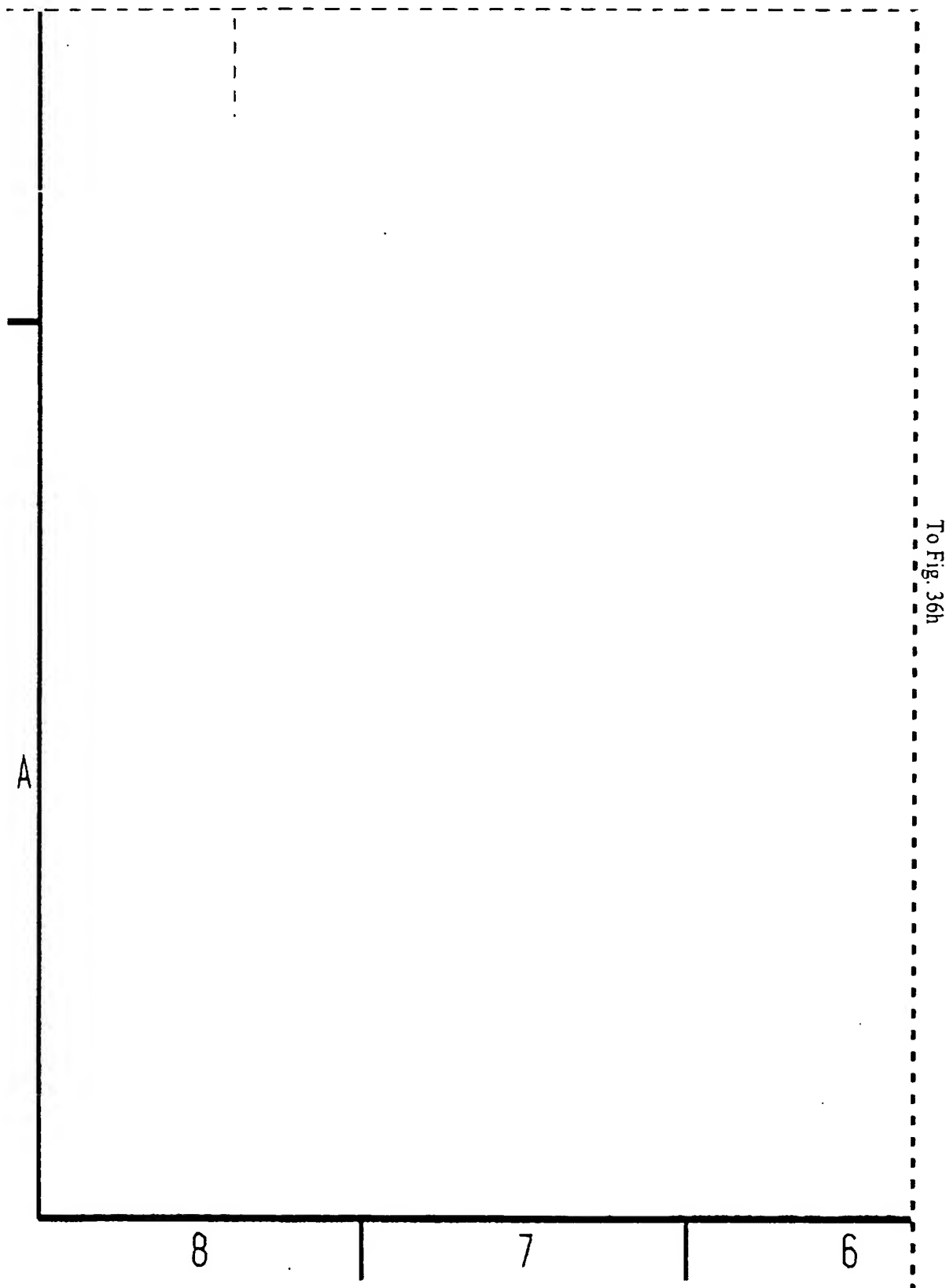
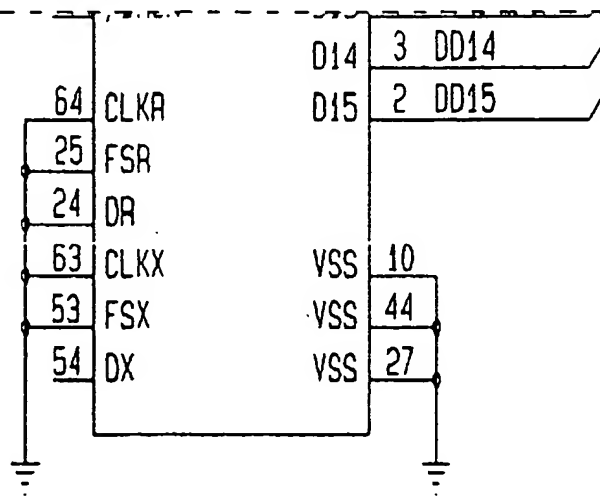


FIG. 36g

116 86 07

To Fig. 36e



To Fig. 36g

To Fig. 36i

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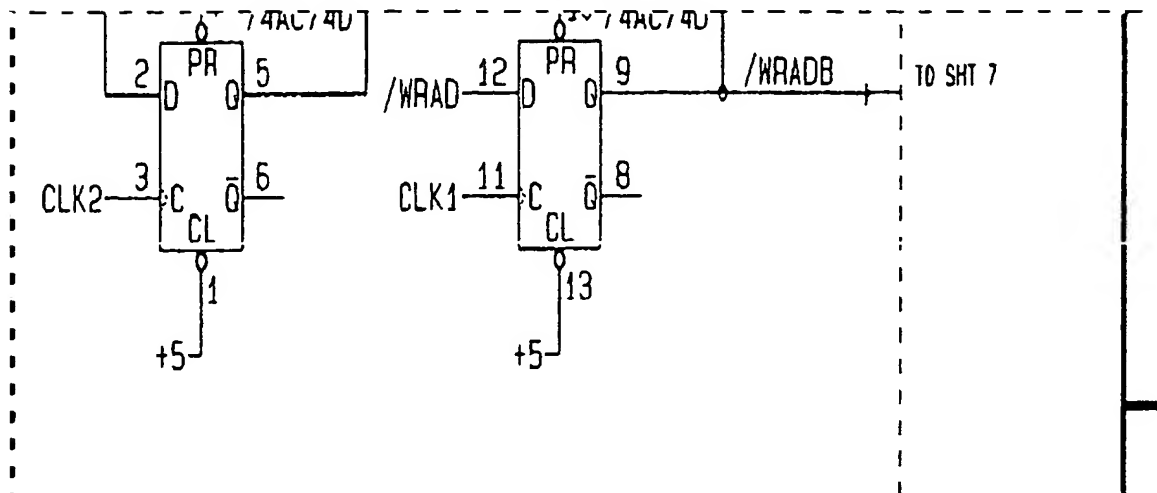
4

FIG. 36h



117 06 207

To Fig. 36f



To Fig. 36h

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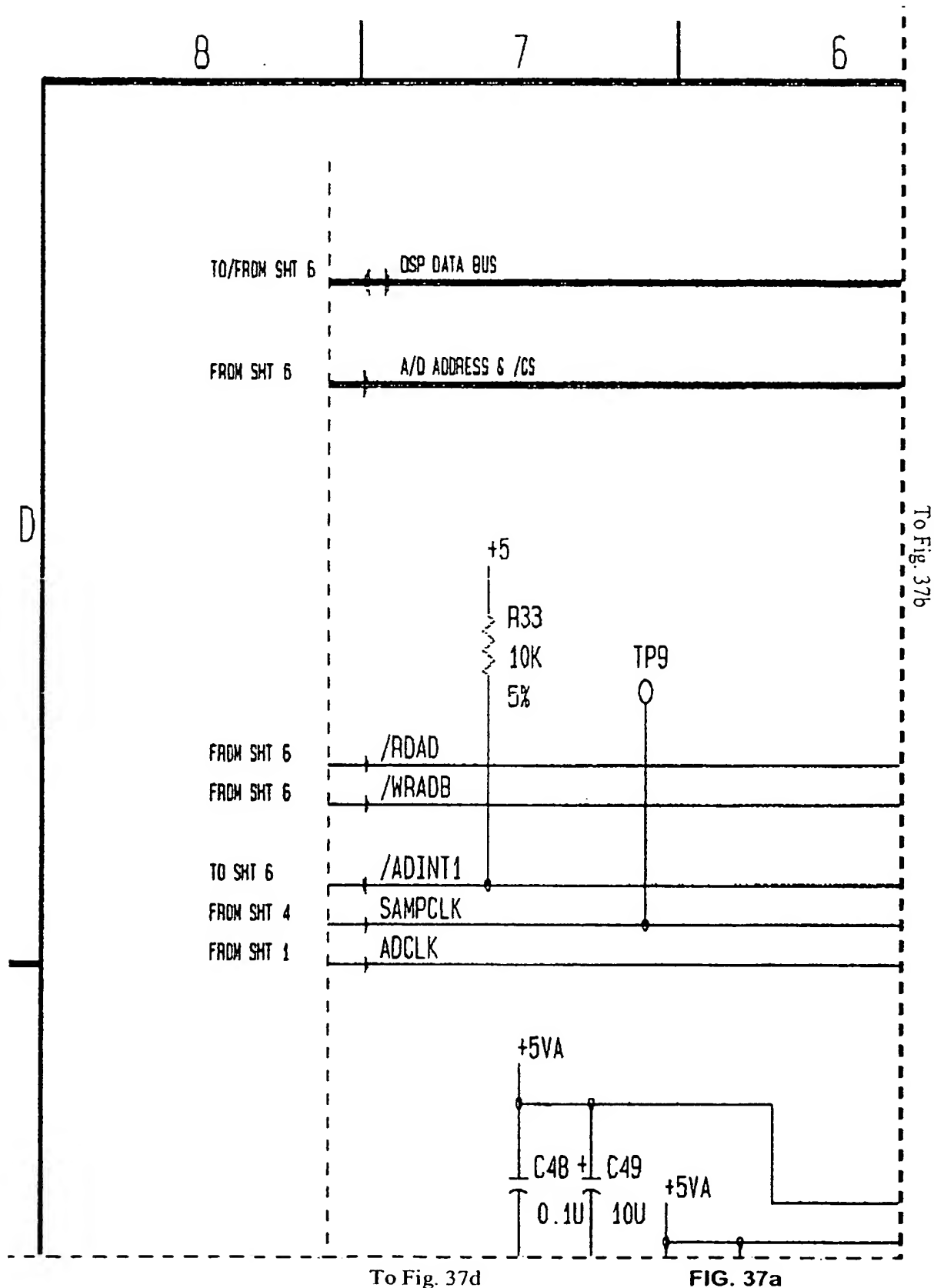
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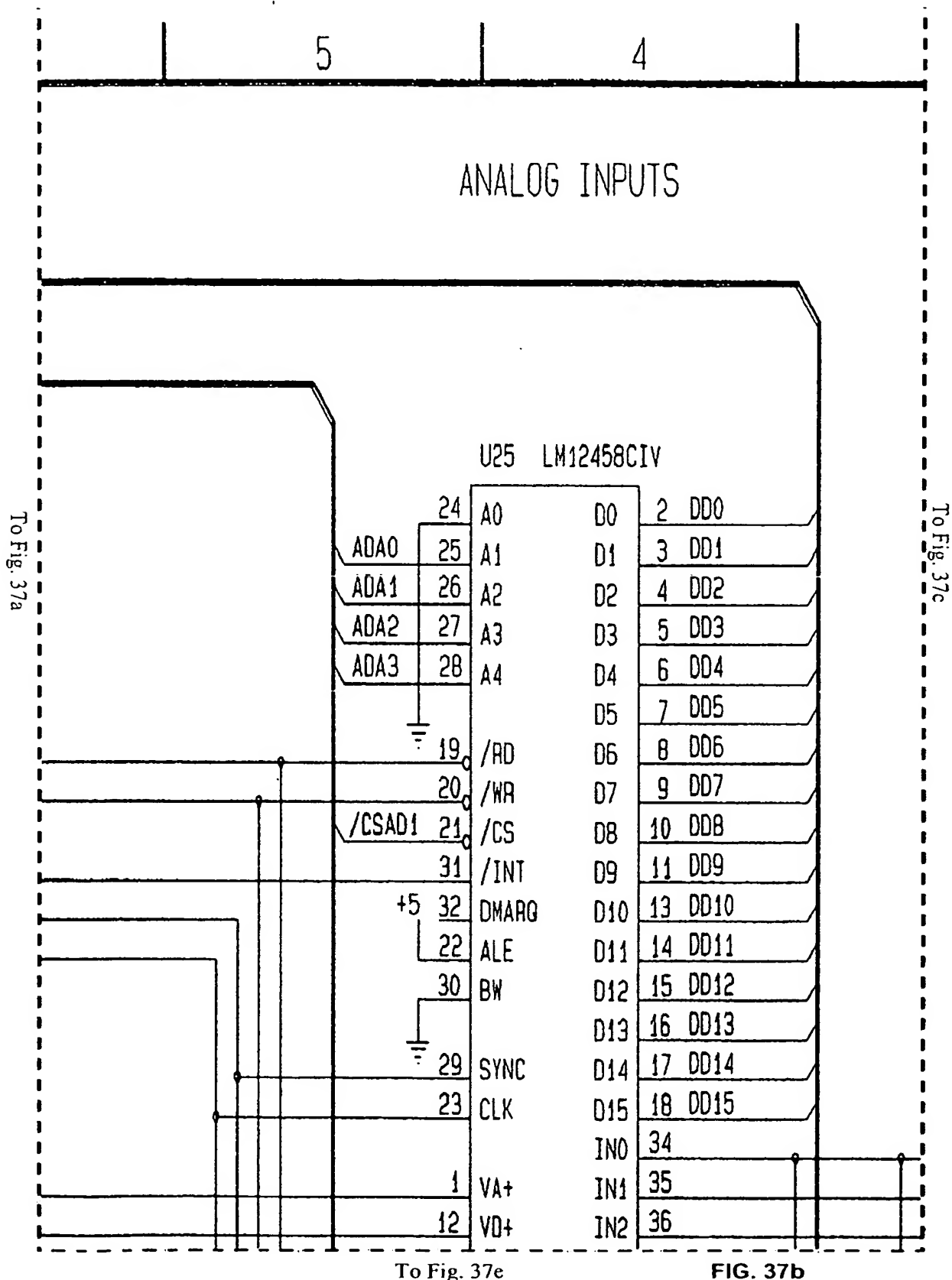
2

1

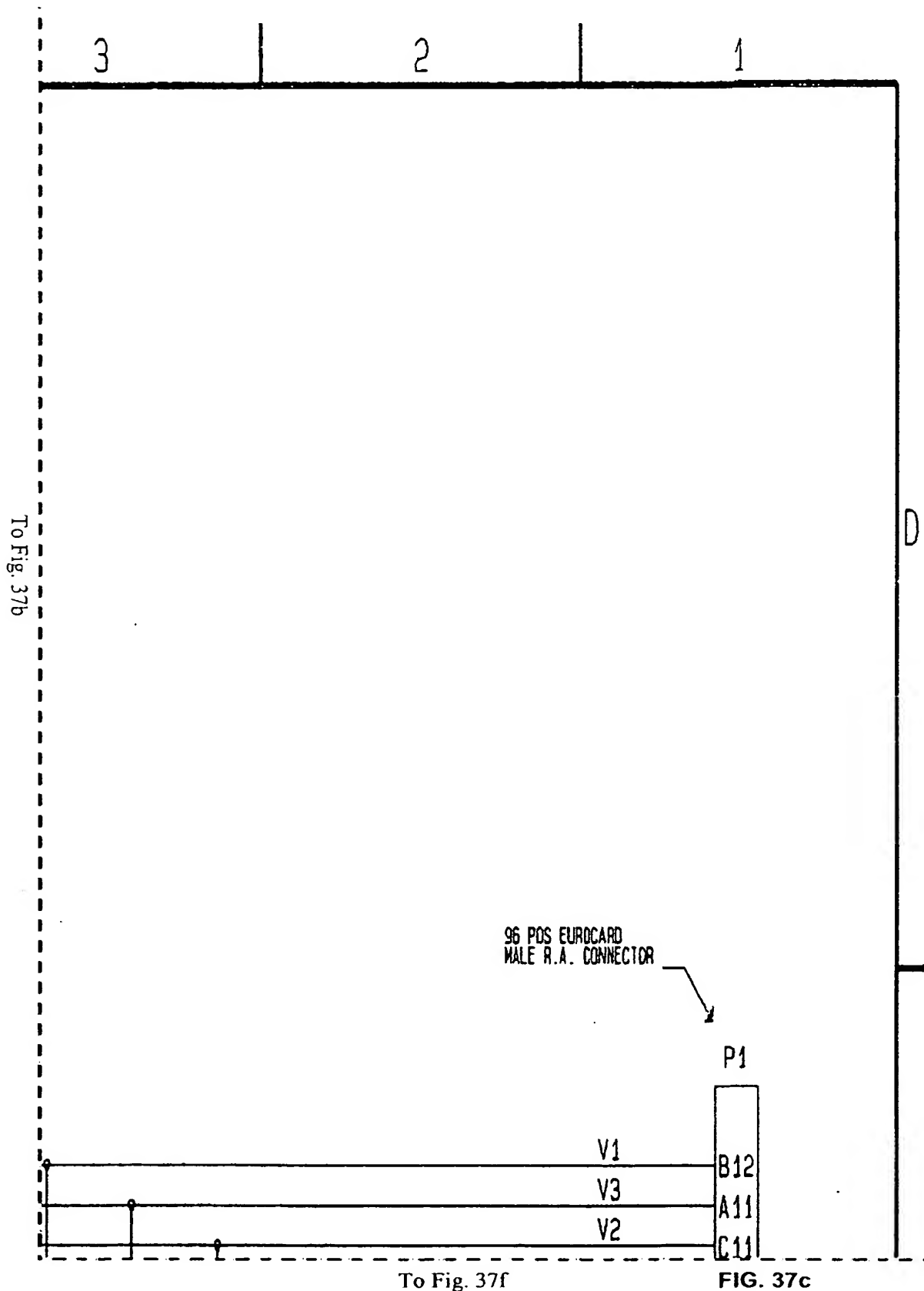
FIG. 36i

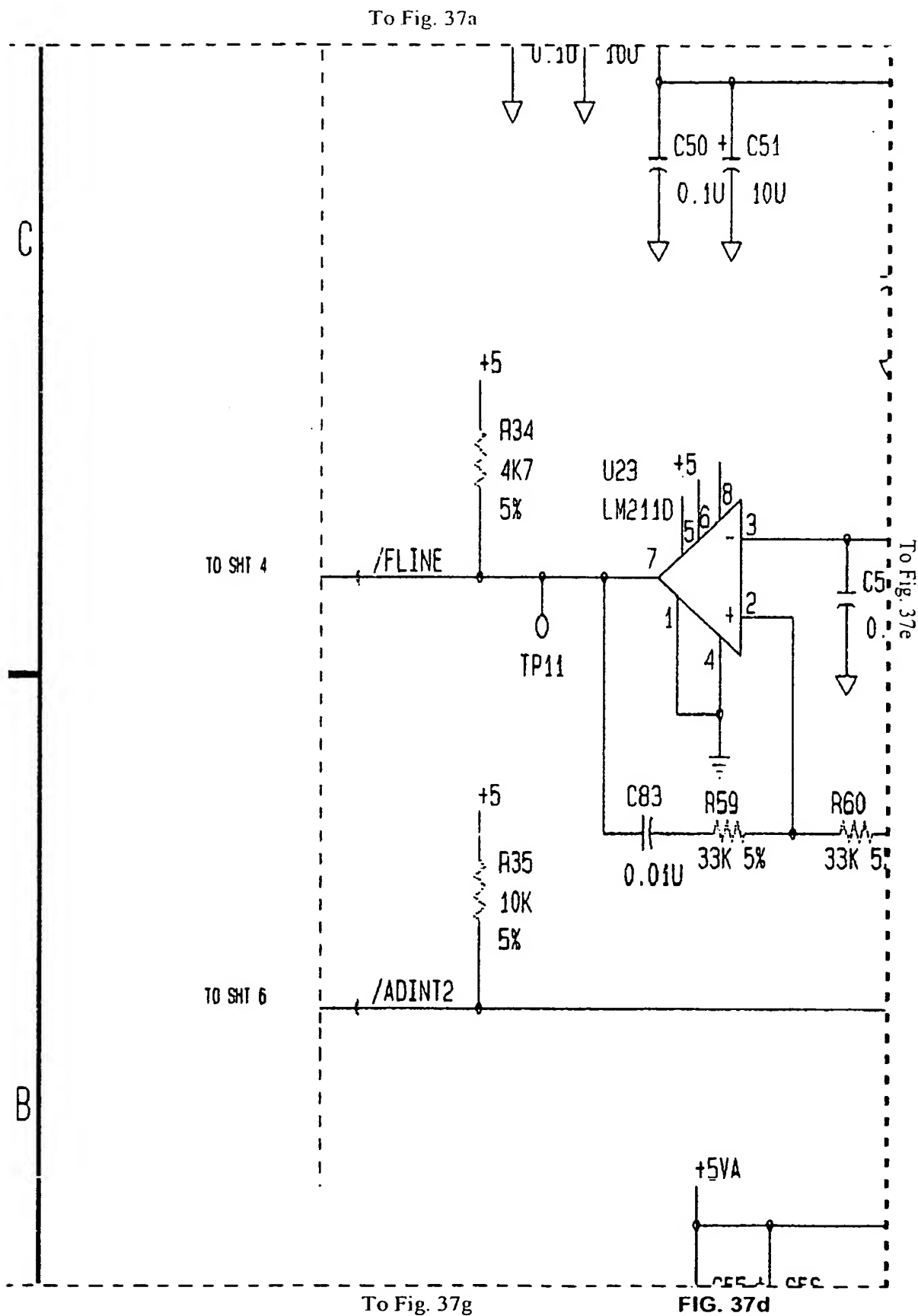
118 0207





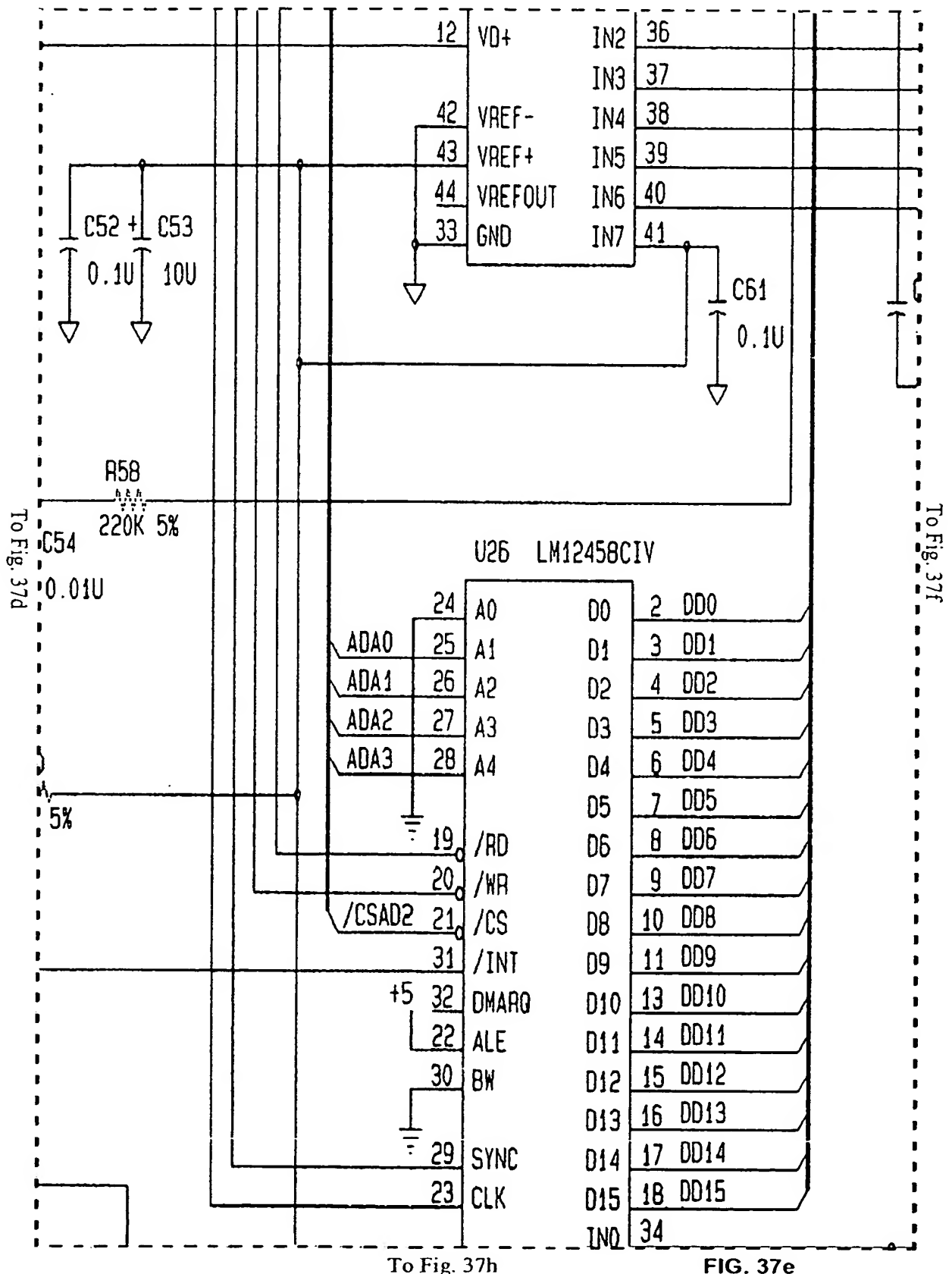
120 89 207





122 06 207

To Fig. 37b

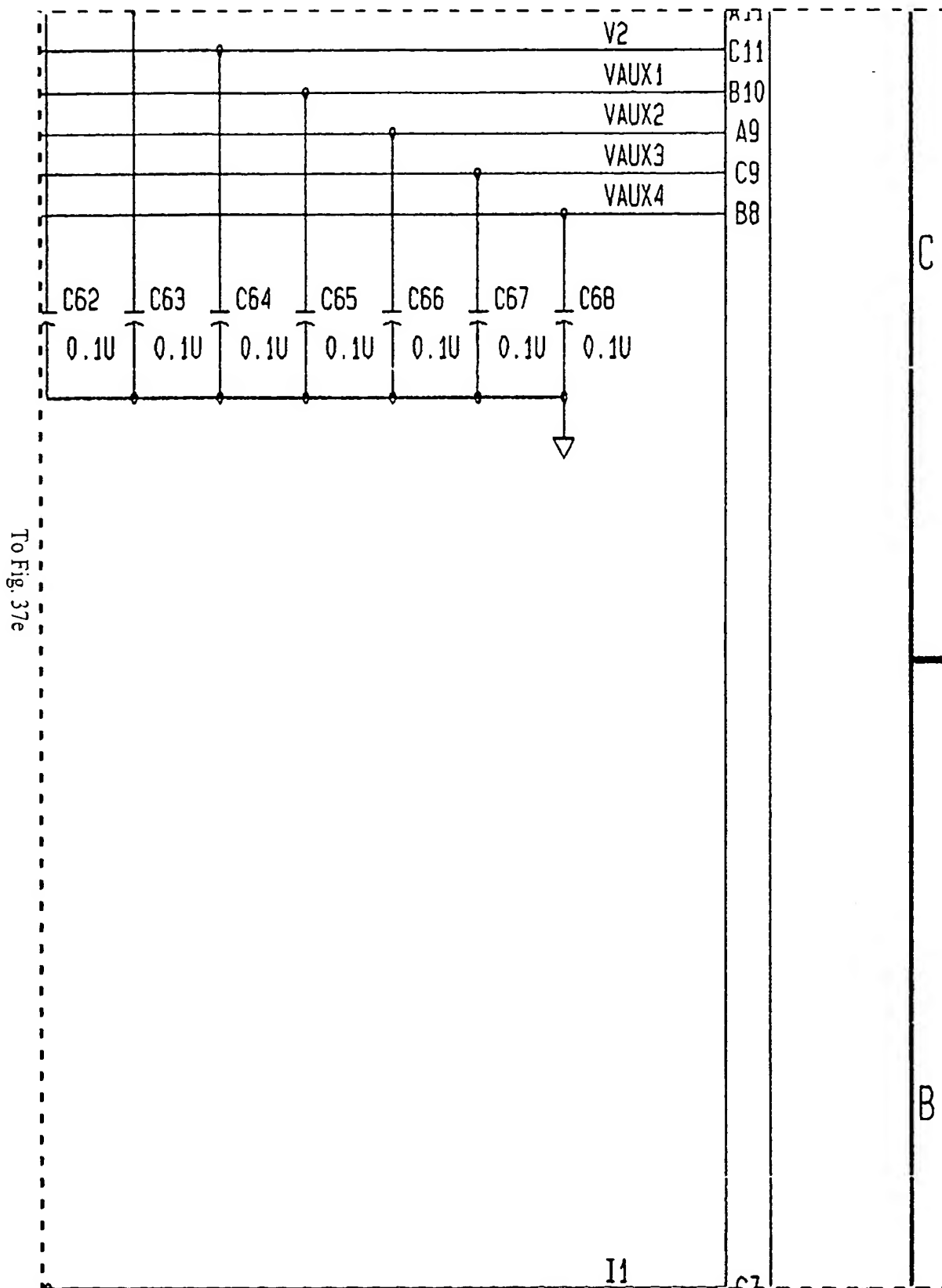


To Fig. 37h

FIG. 37e

123 08 207

To Fig. 37c



To Fig. 37i

FIG. 37f

124 8 207

To Fig. 37d

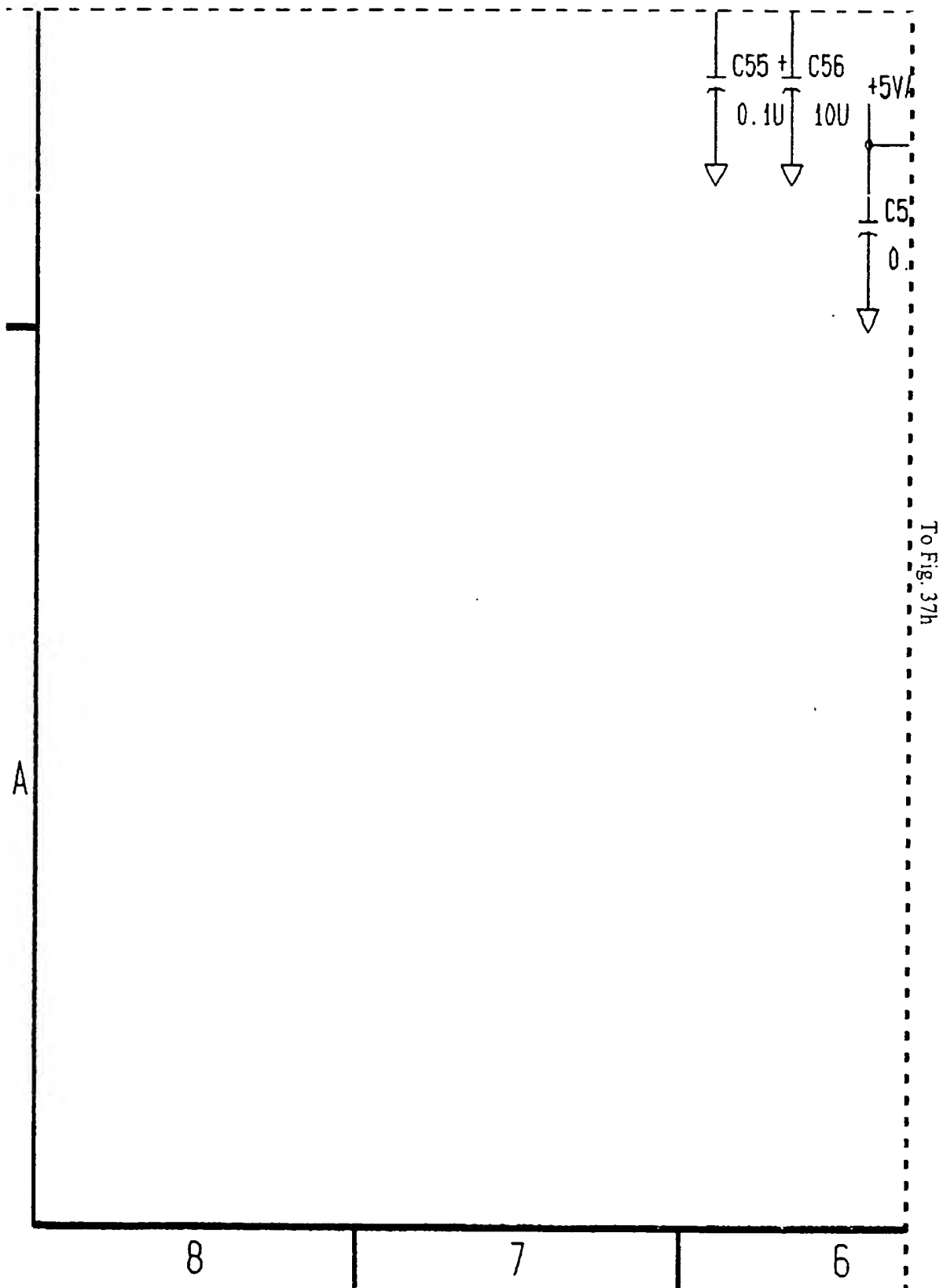


FIG. 37g



Schematic diagram of the AD7714 ADC converter. The device is shown with its pins and internal connections. Pin 1 is VA+, pin 12 is VD+, pin 42 is VREF-, pin 43 is VREF+, pin 44 is VREFOUT, and pin 33 is GND. The internal connections show the reference voltage divider network. A capacitor C69 is connected between the VREF+ pin and ground, with a value of 0.1uF.

To Fig. 37g

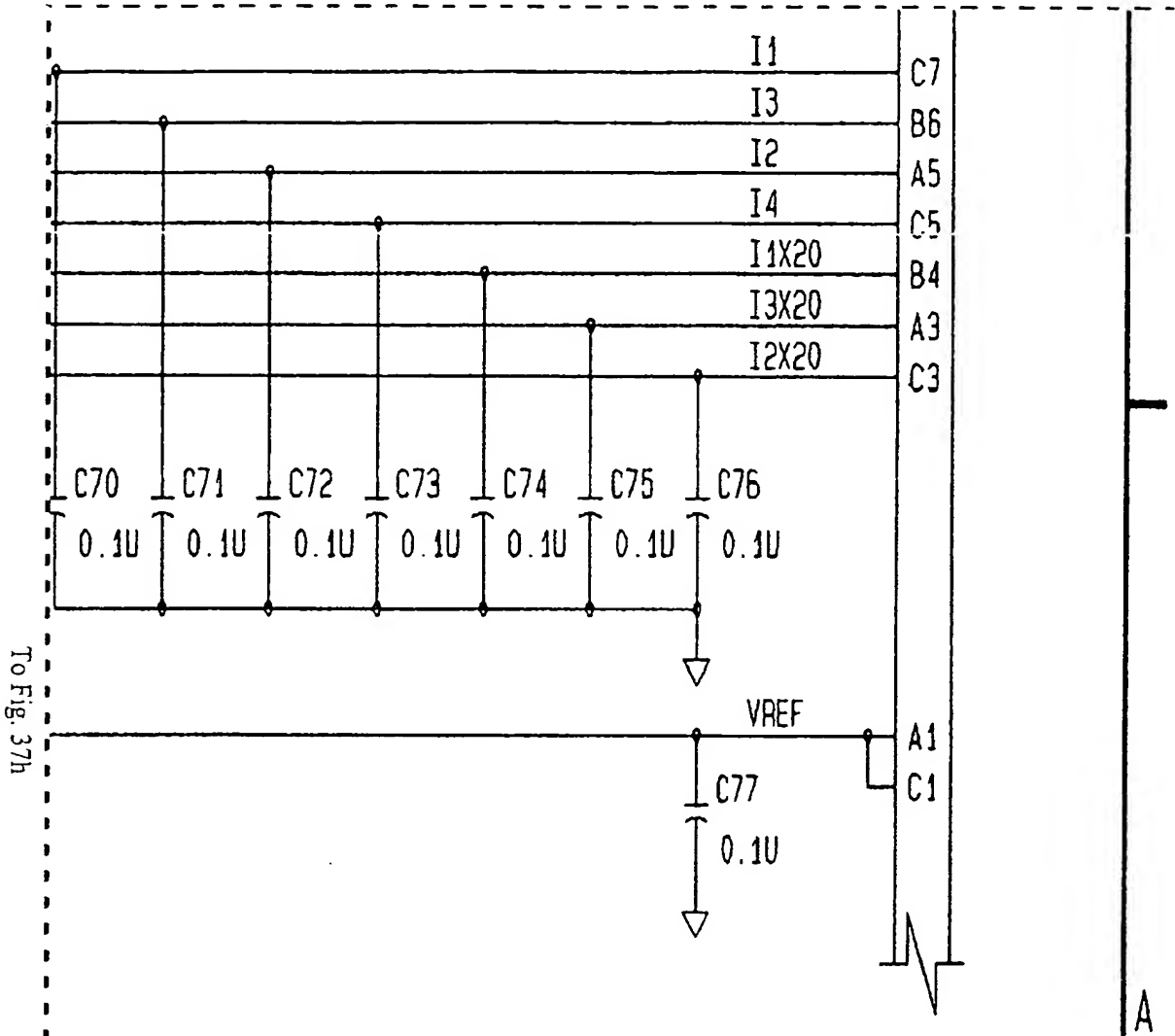
To Fig. 37i

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FIG. 37h

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To Fig. 37f



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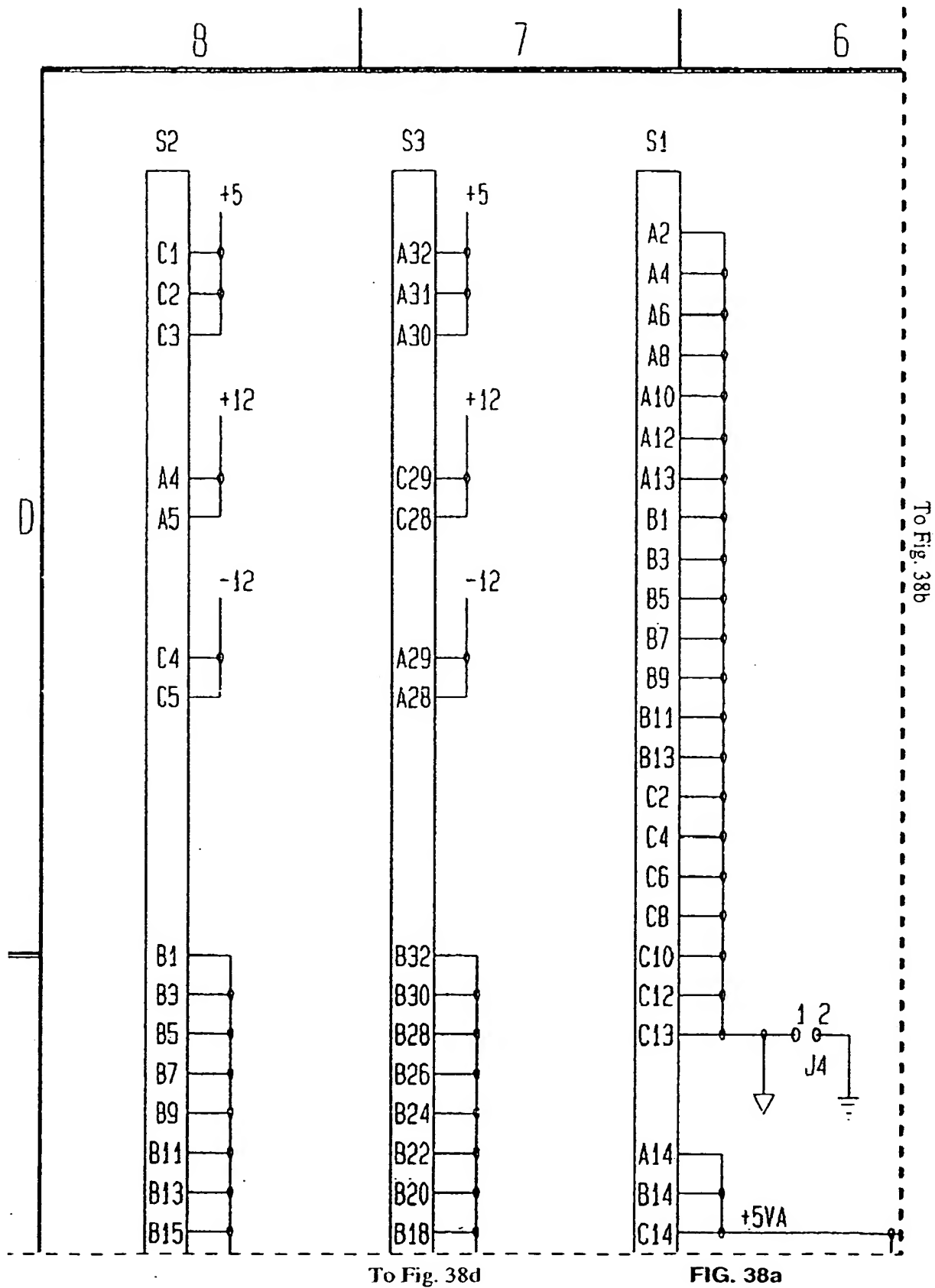
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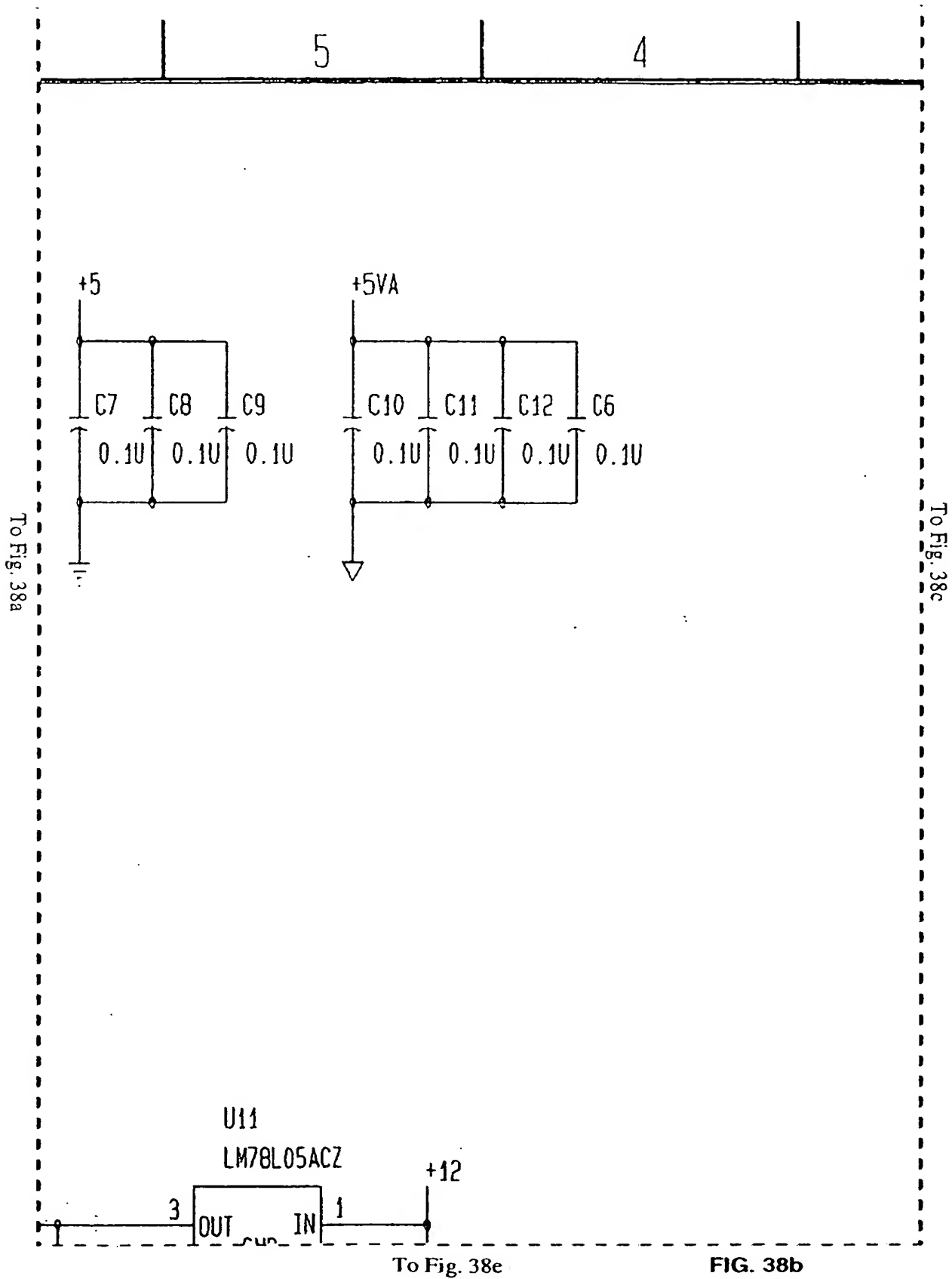
1

FIG. 37i

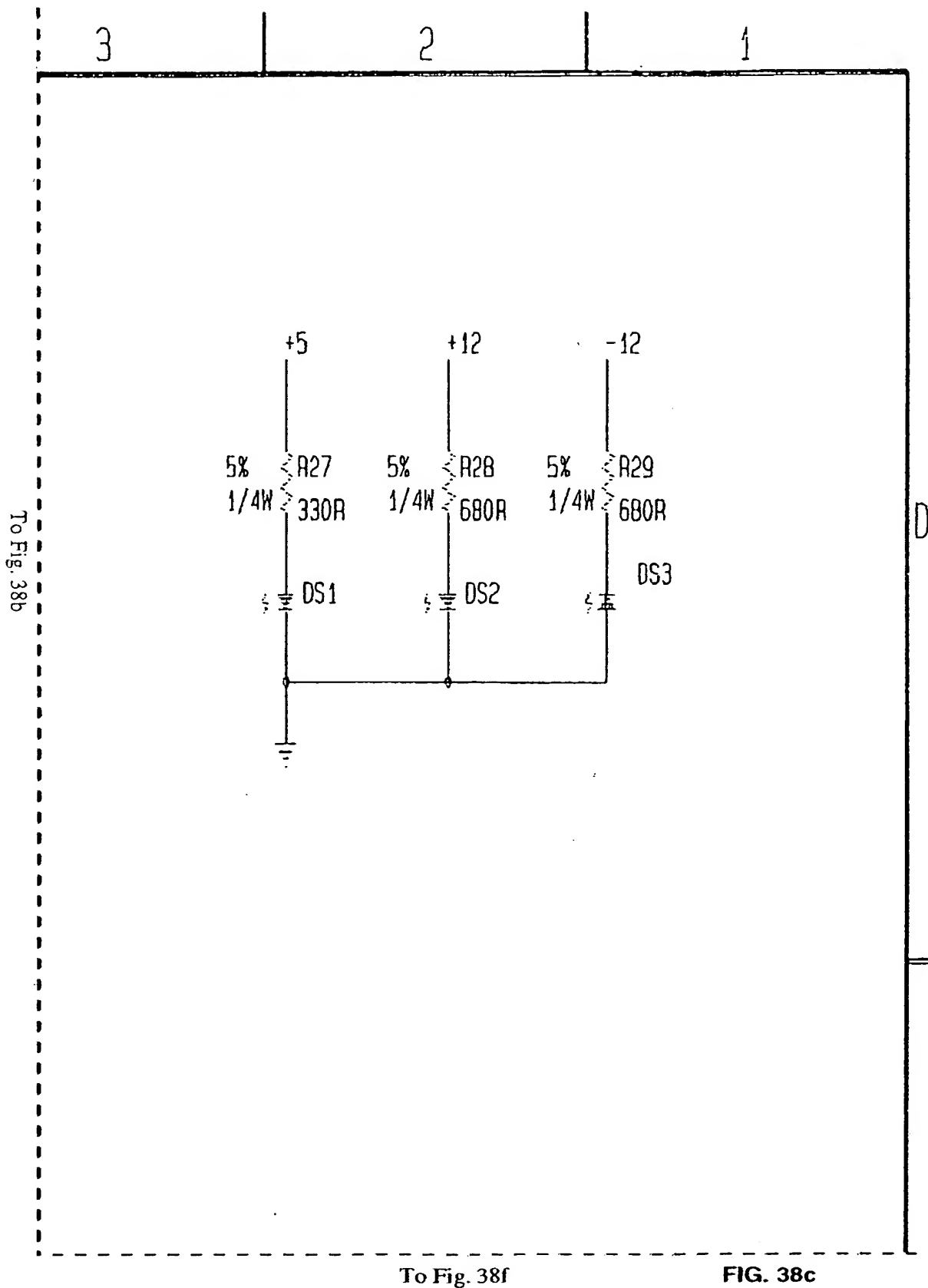
127 8 307



128 9 207

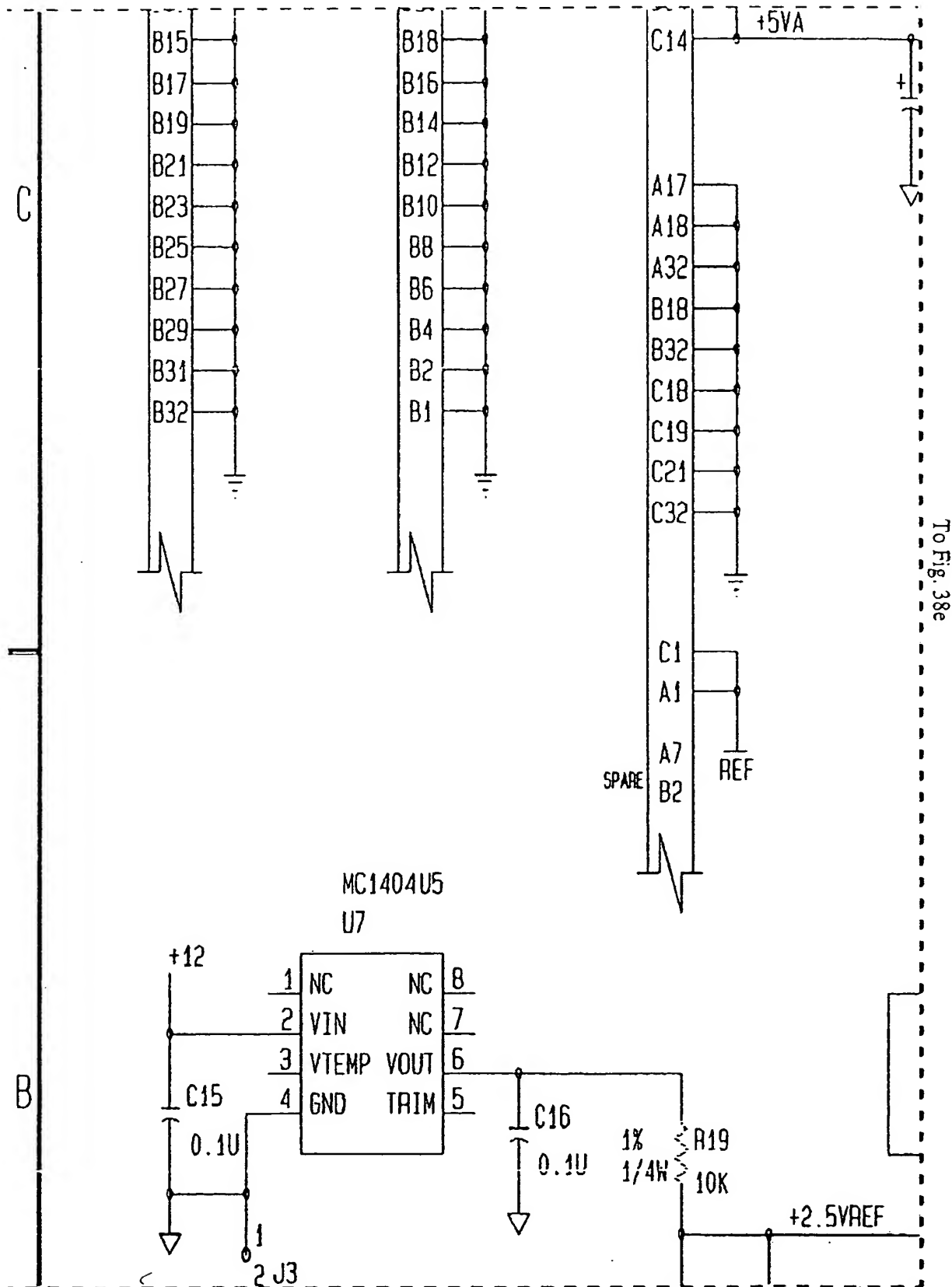


129 8 207



130 08207

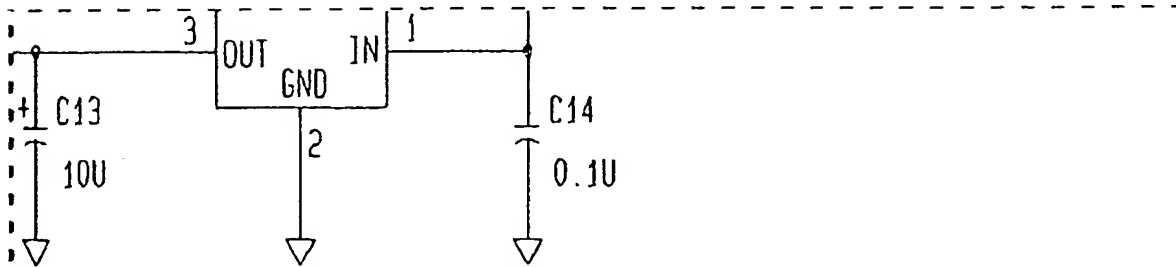
To Fig. 38a



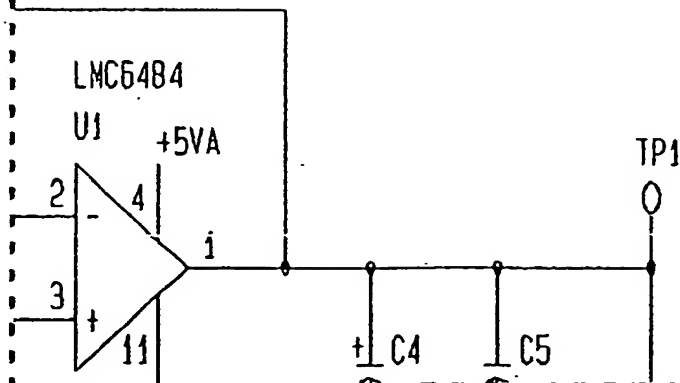
To Fig. 38g

FIG. 38d

To Fig. 38b



To Fig. 38f



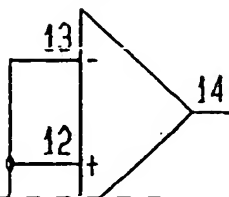
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To Fig. 38c

To Fig. 38e

SPARES

LMC6484  
U10



To Fig. 38i

FIG. 38f

C

B



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To Fig. 38d

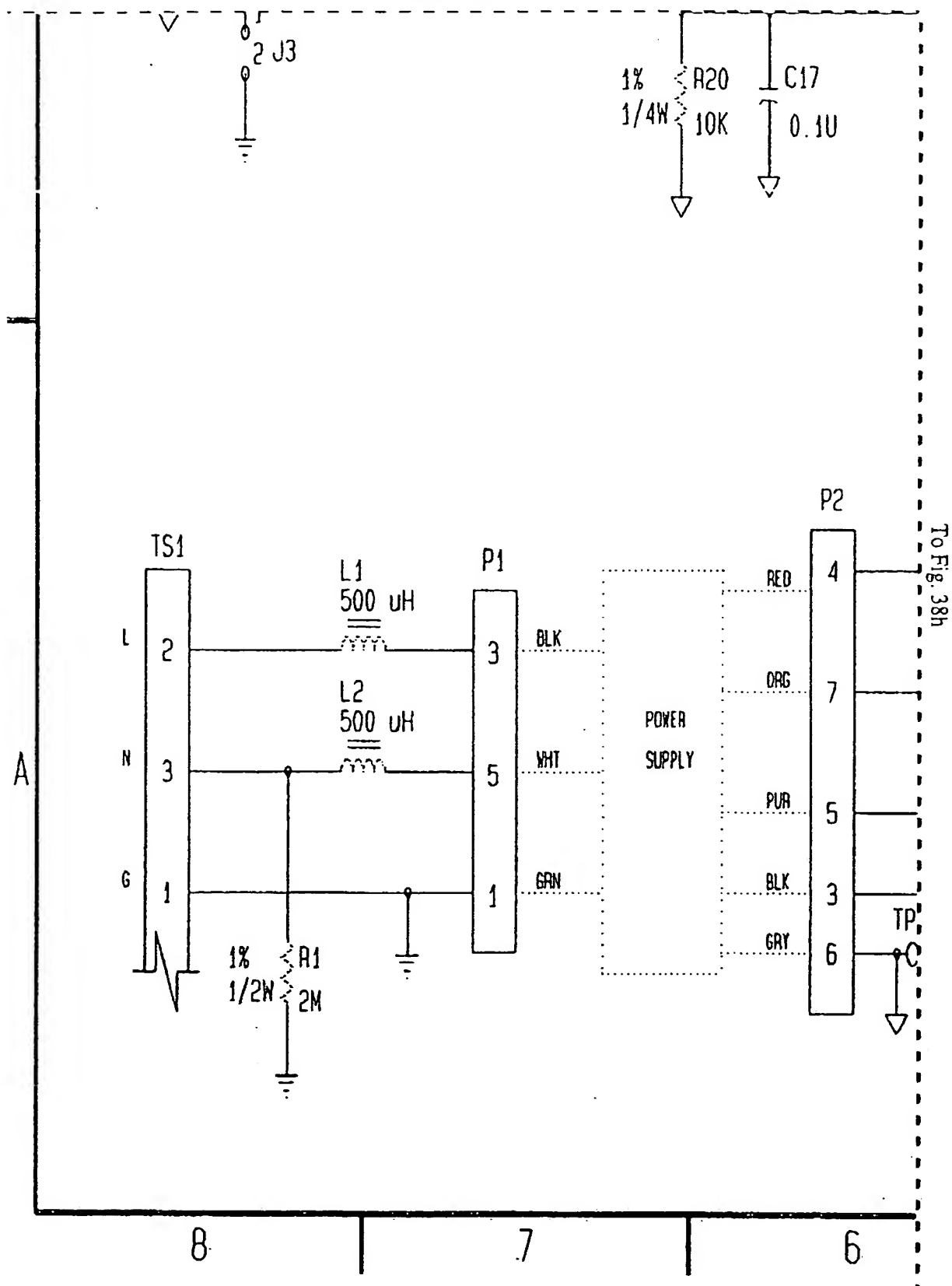
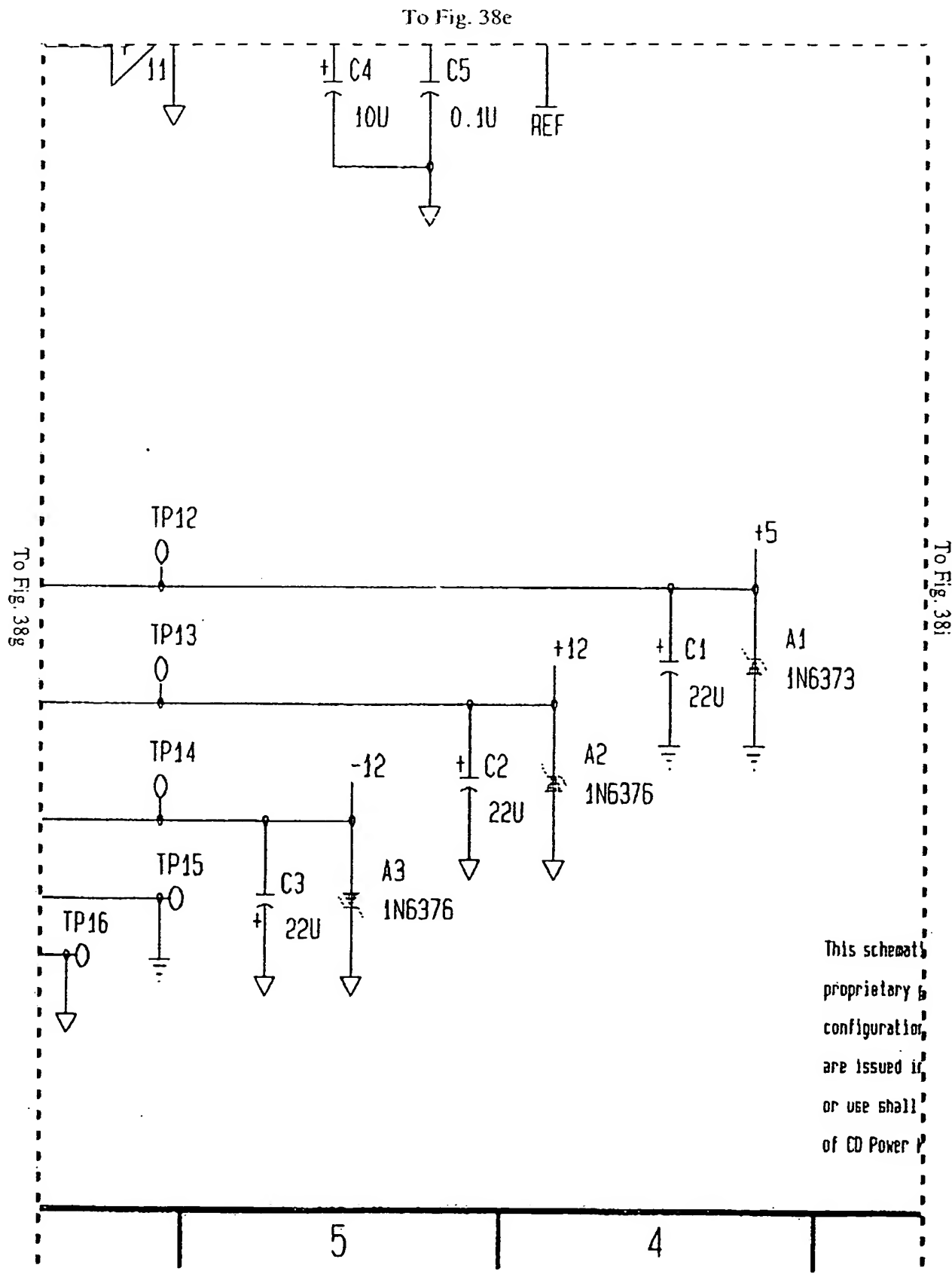


FIG. 38g

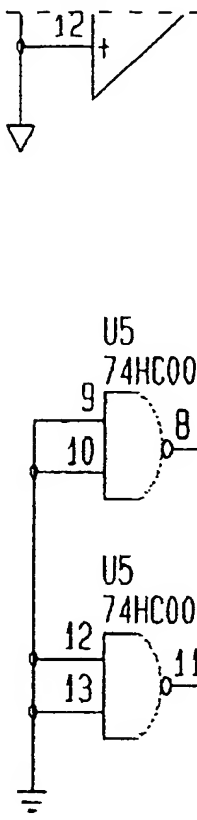
134 8 207



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To Fig. 38f

To Fig. 38h



LAST USED: U11  
 R39  
 C30  
 S6  
 P4  
 A16  
 DS3  
 TP16  
 J5  
 PIC3  
 TS3  
 L2  
 T4

A

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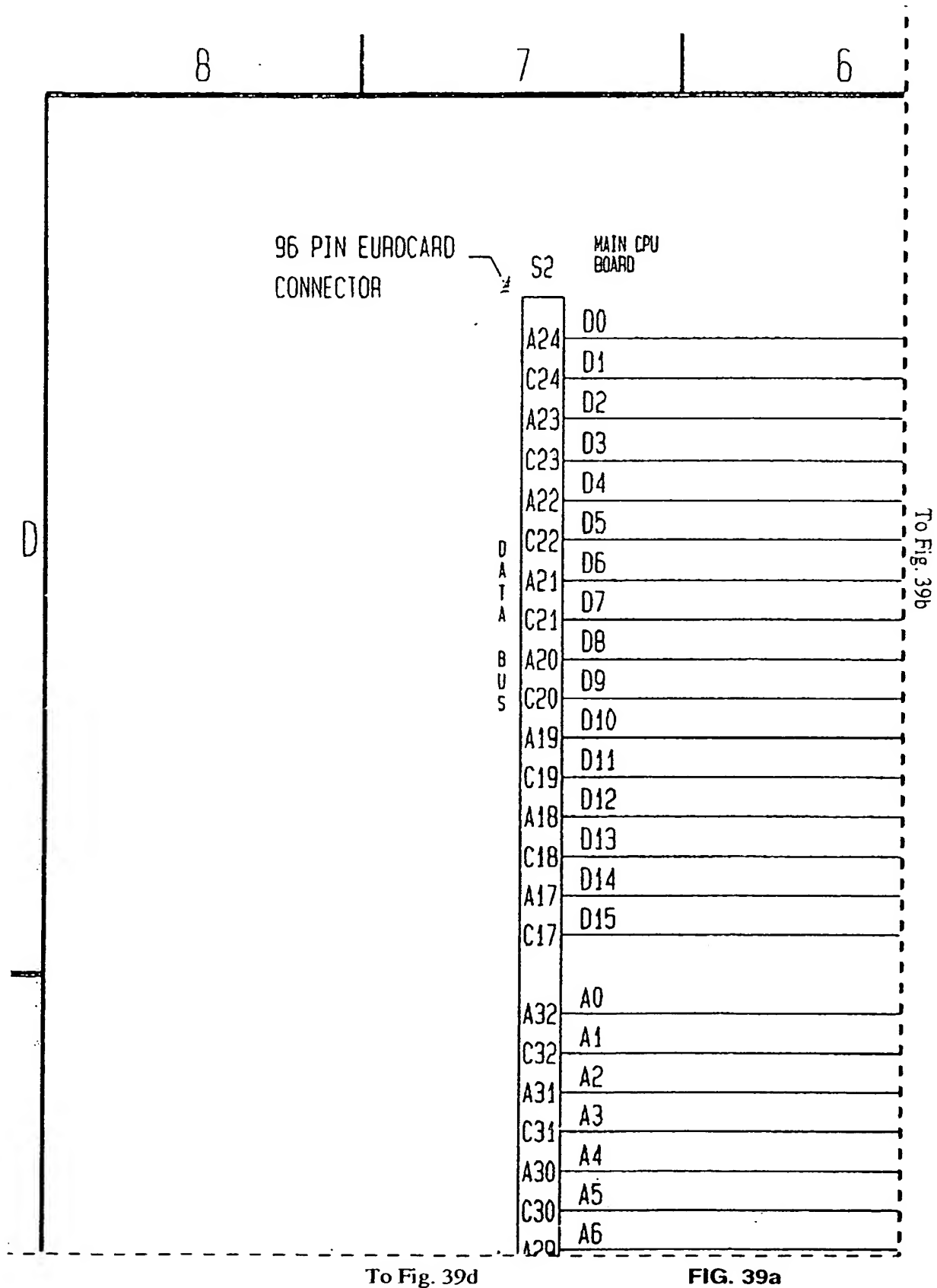
3

2

1

FIG. 38i

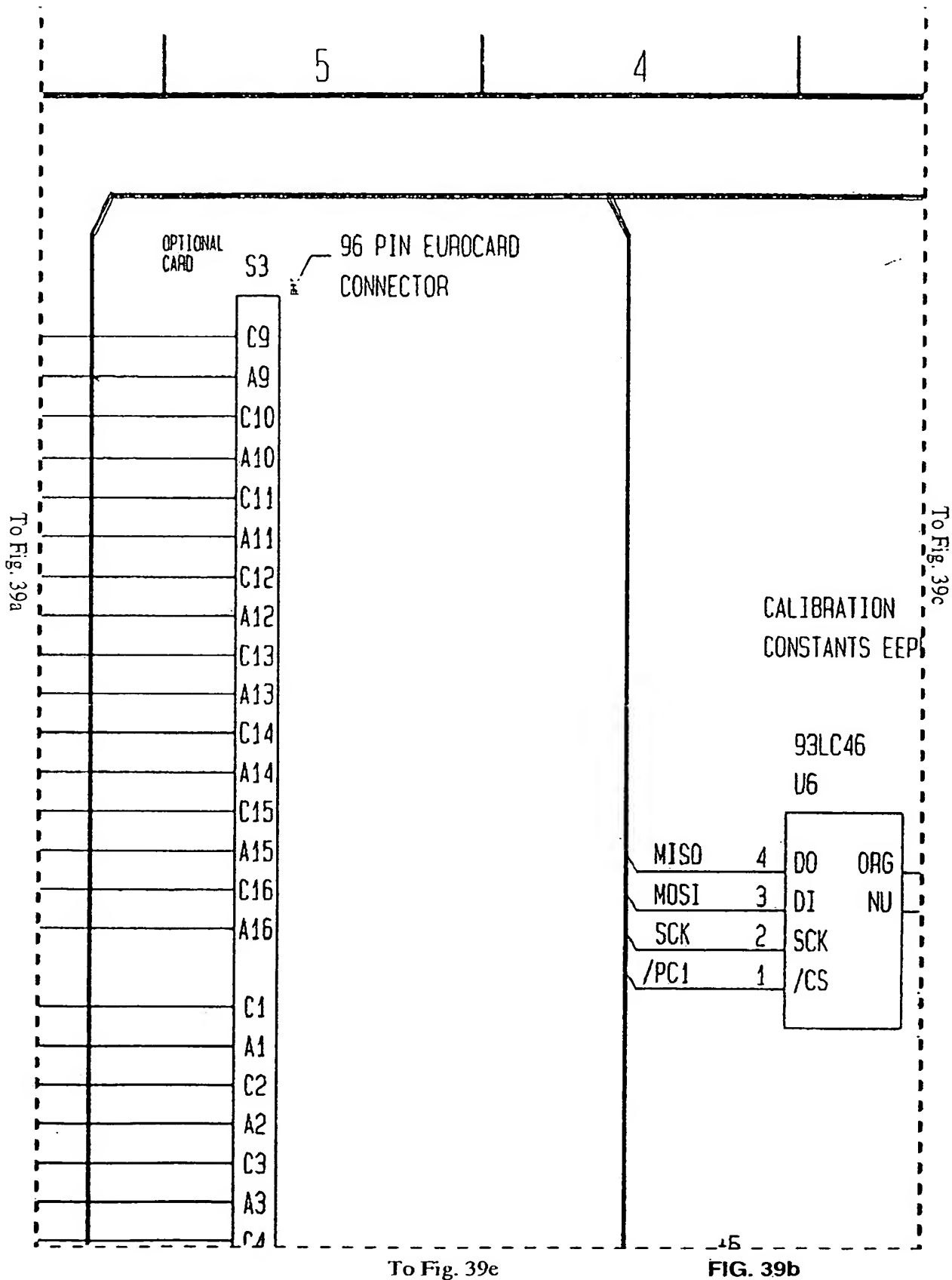
136 08 207



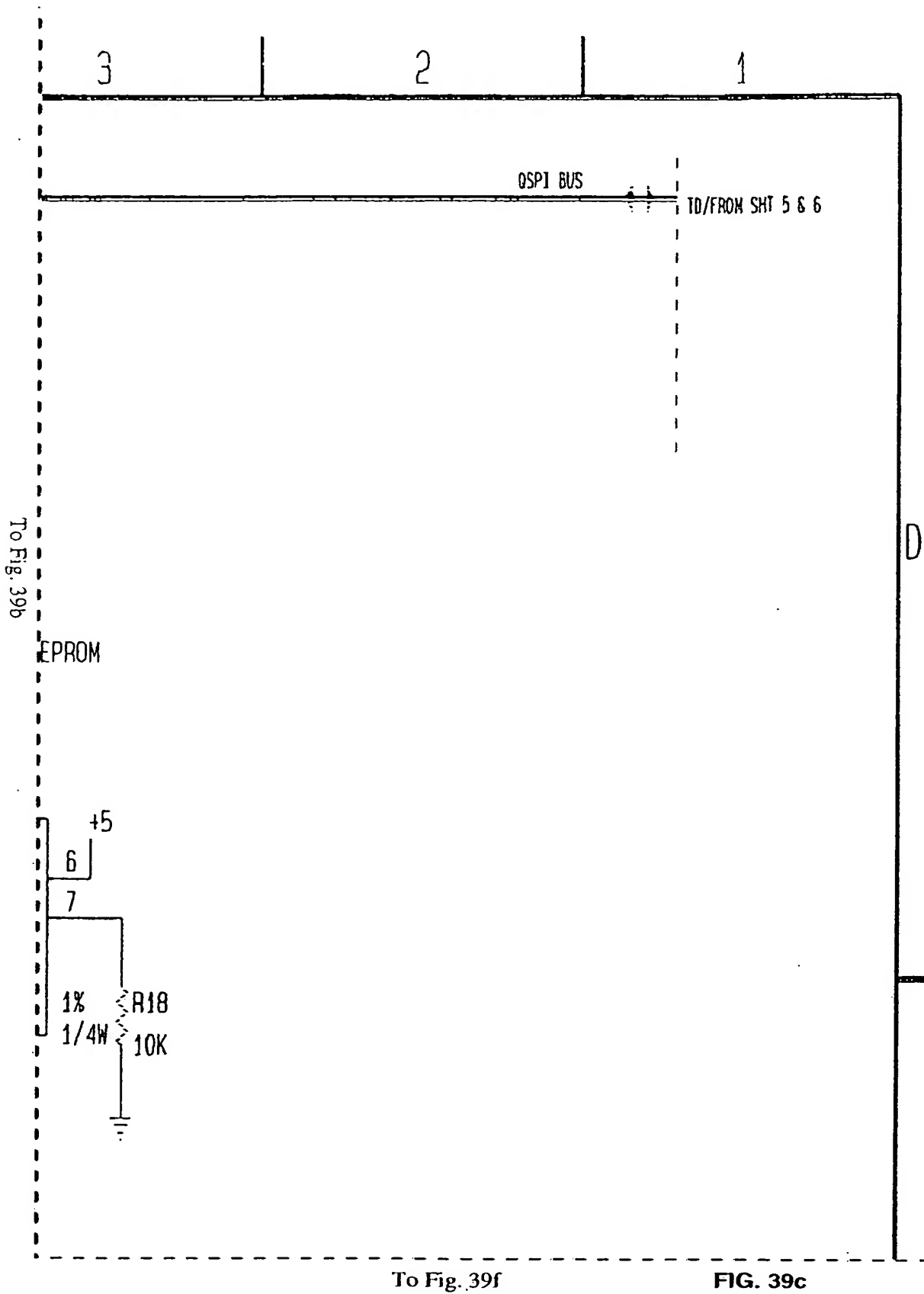
To Fig. 39d

FIG. 39a

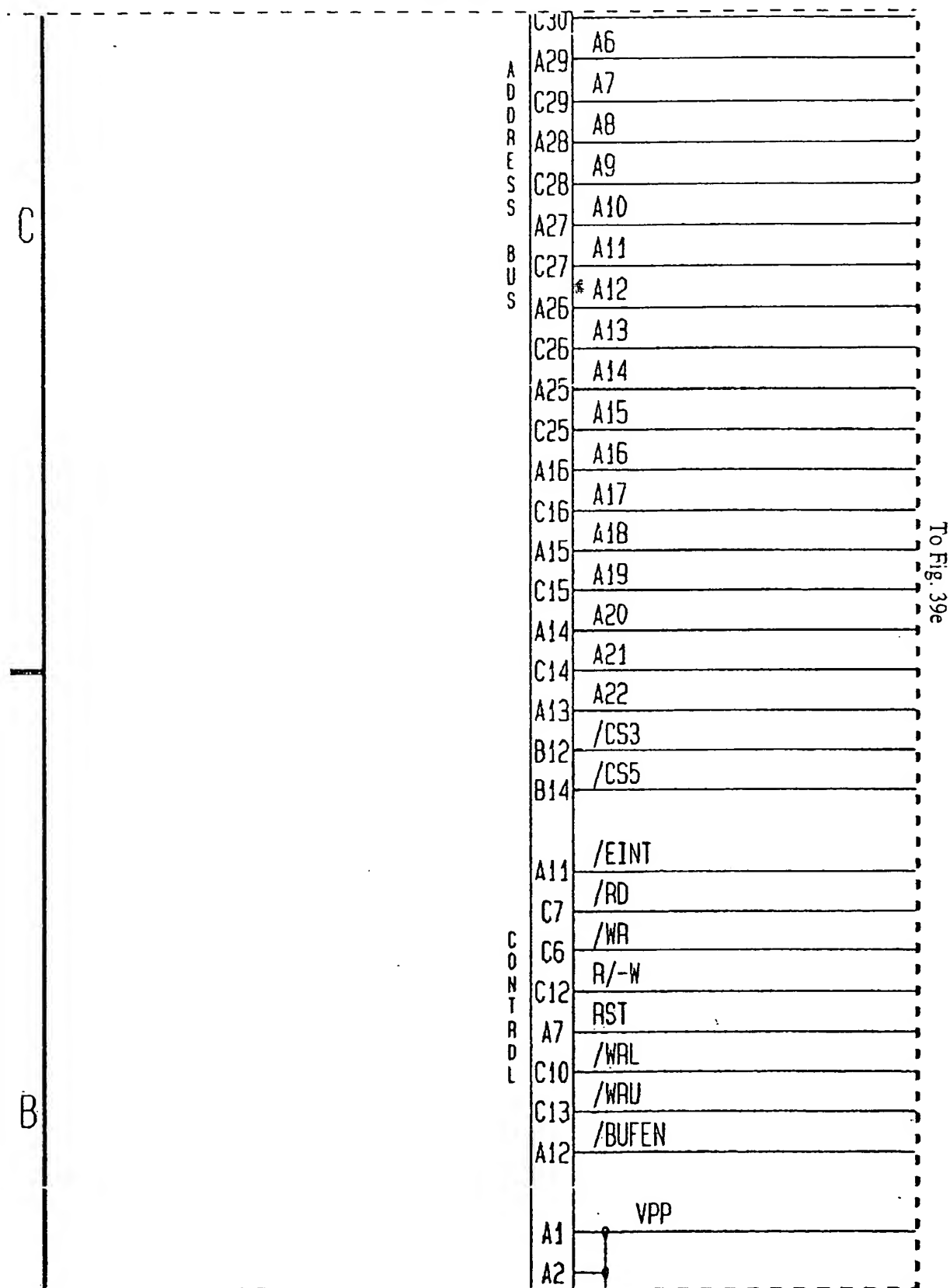
13707 207



138 08 207



To Fig. 39a

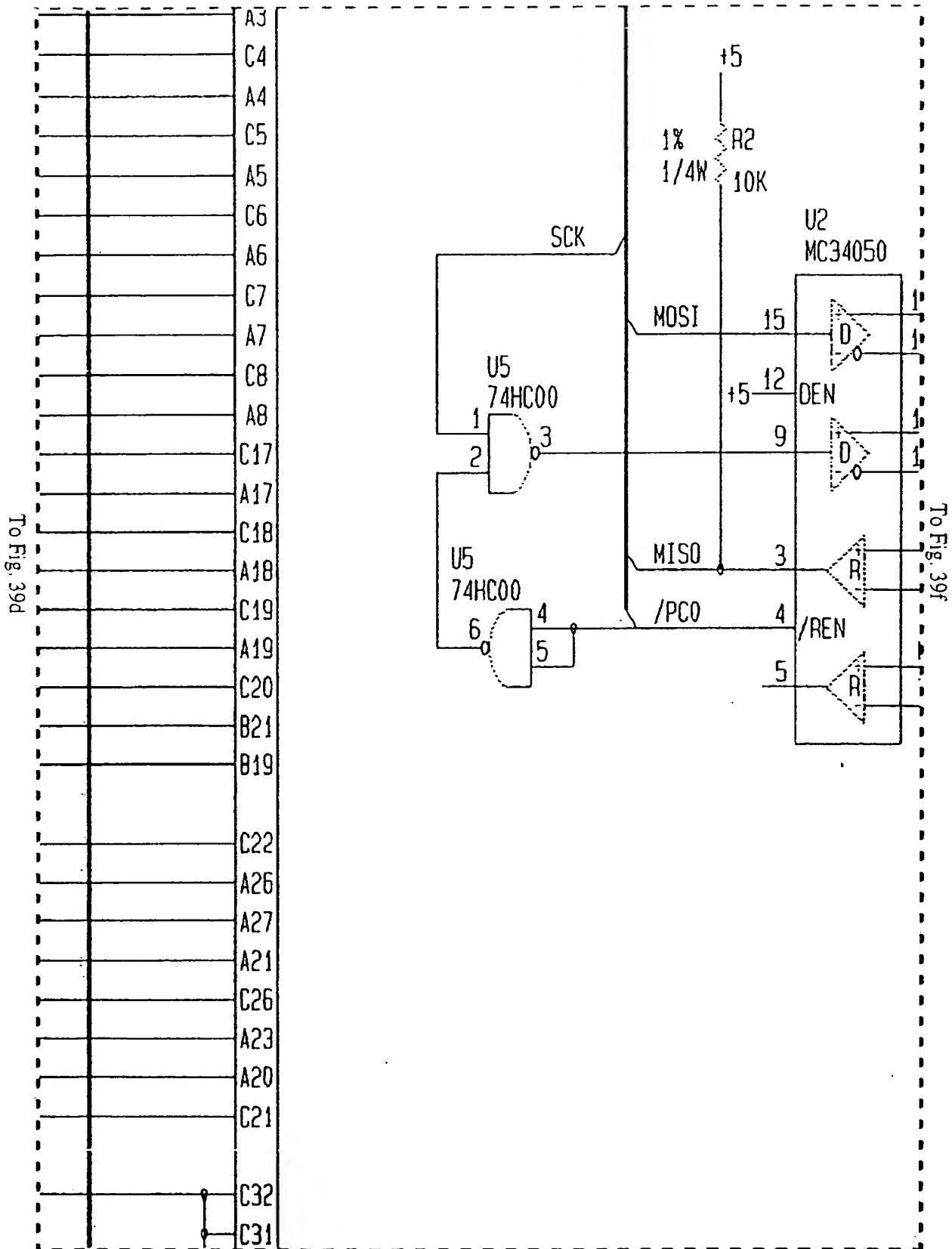


To Fig. 39g

FIG. 39d

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To Fig. 39b



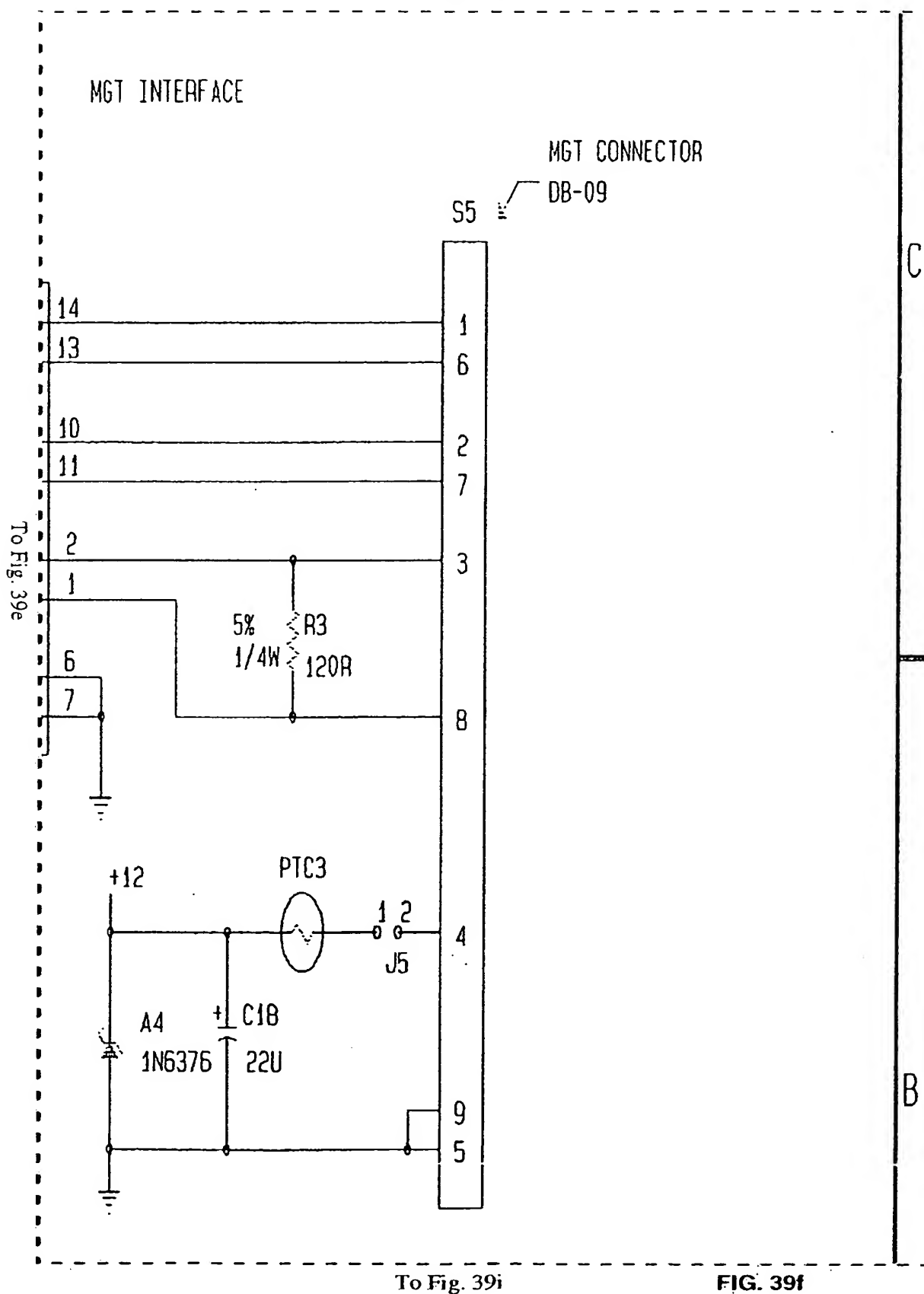
To Fig. 39h

FIG. 39e



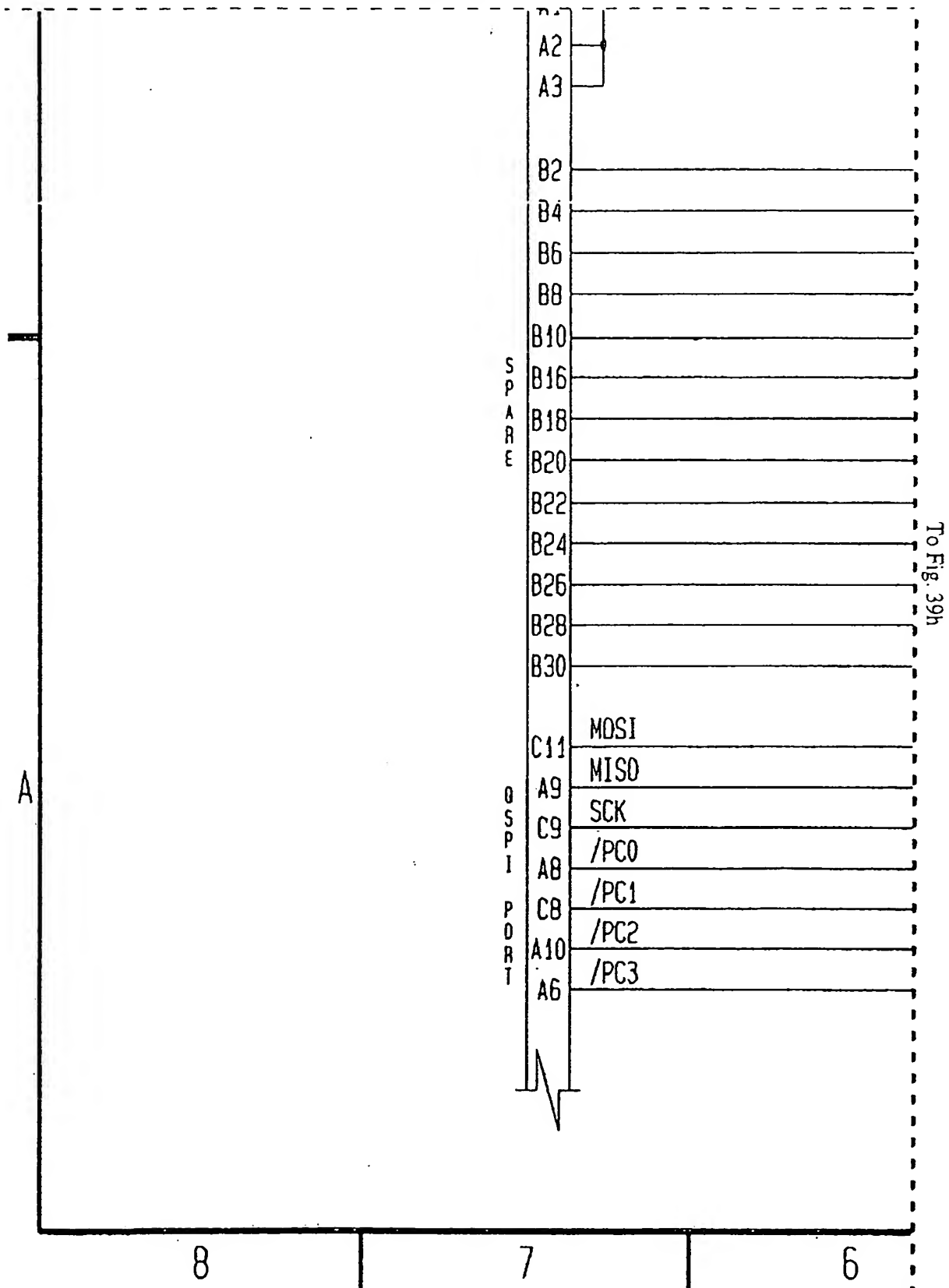
141 a 207

To Fig. 39c



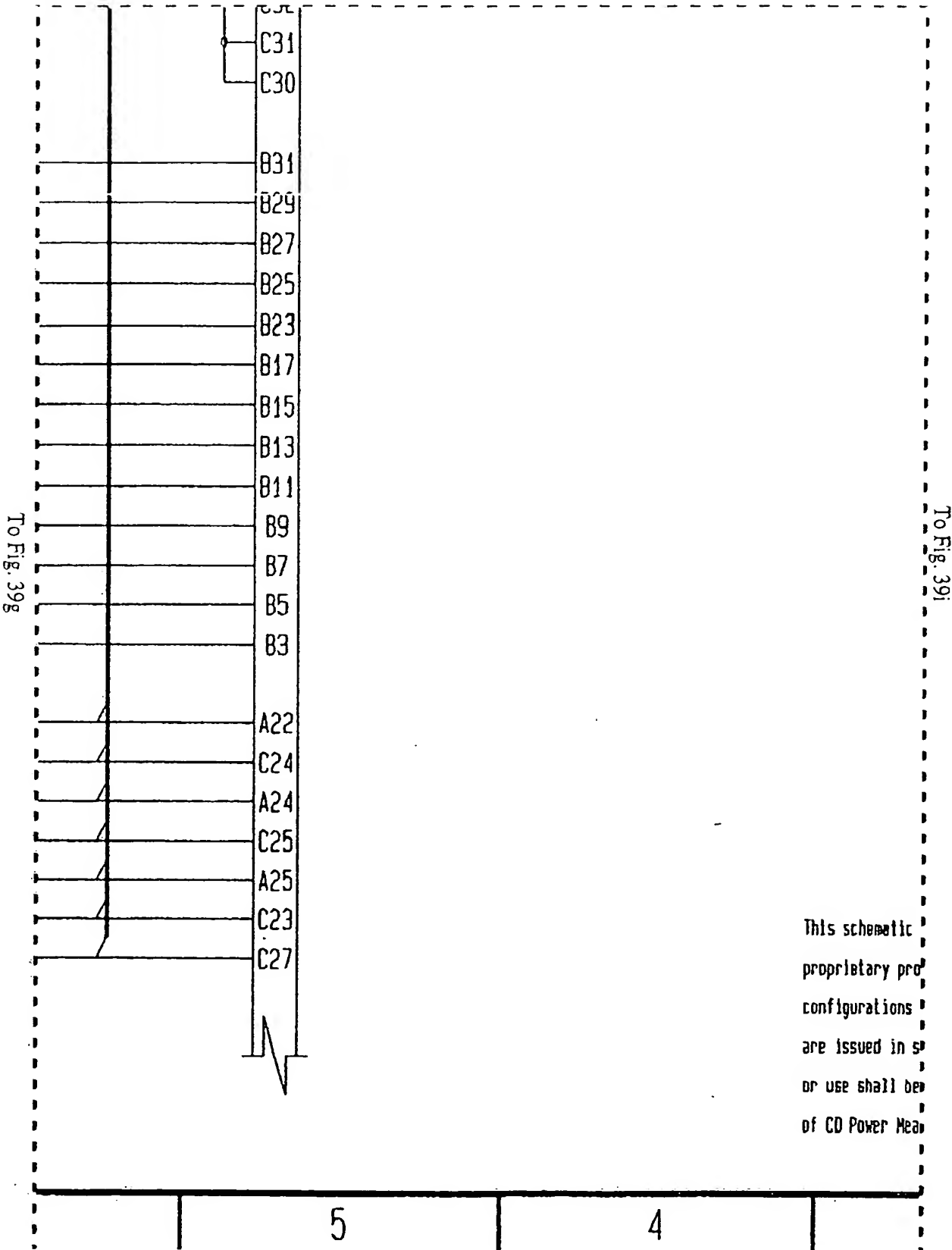
142 08207

To Fig. 39d



143 8207


To Fig. 39e



To Fig. 39f

To Fig. 39h

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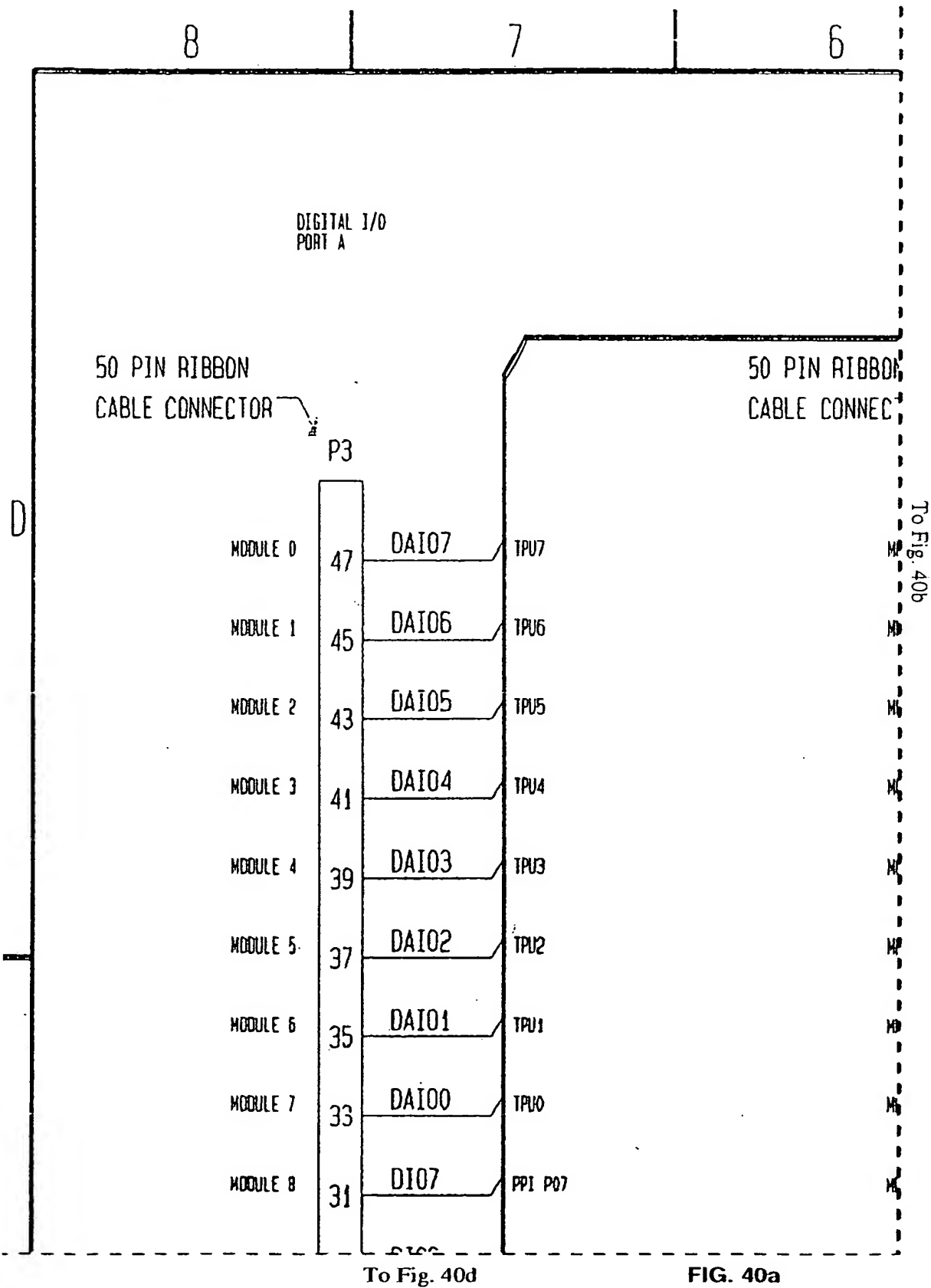
3

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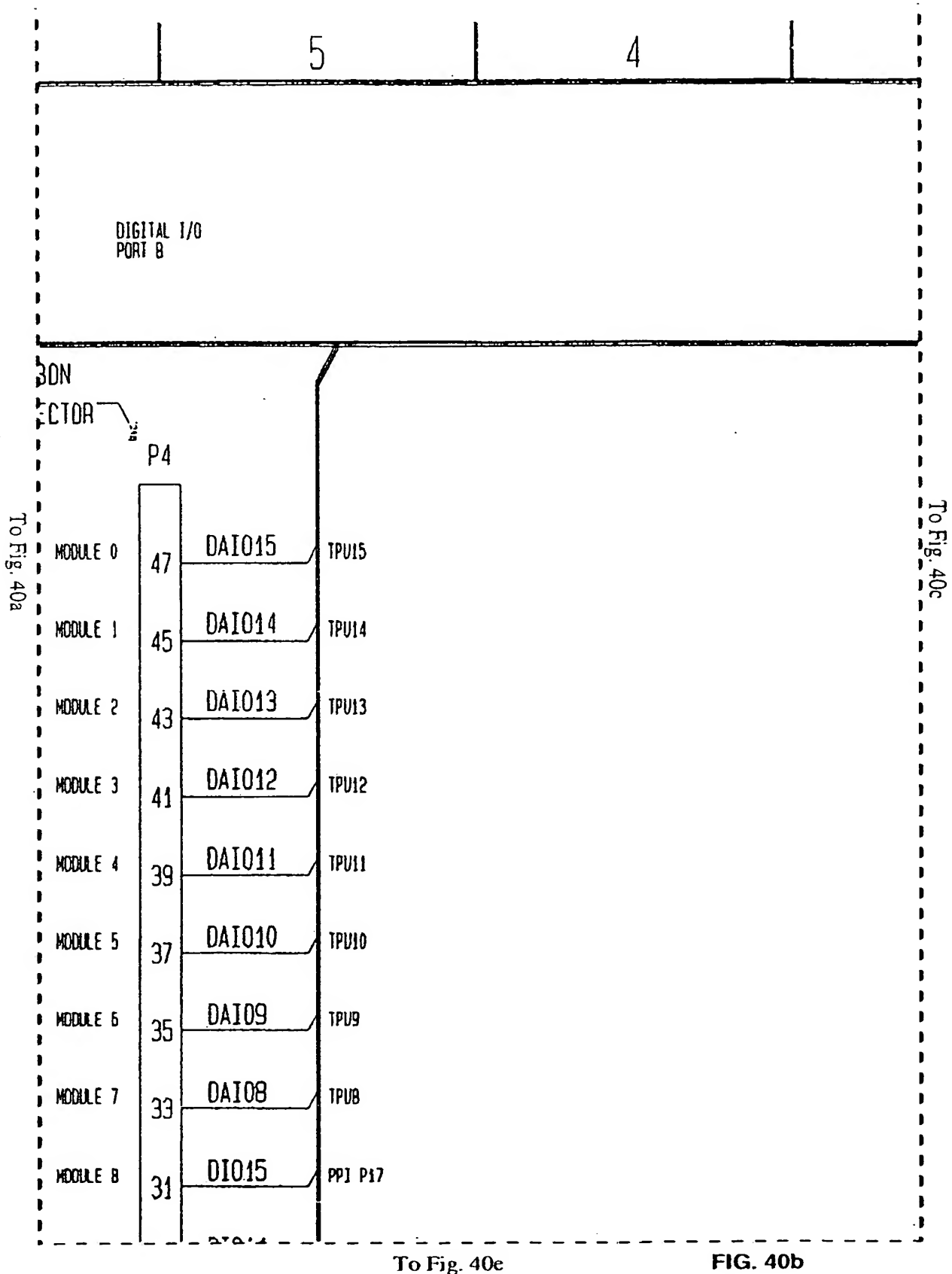
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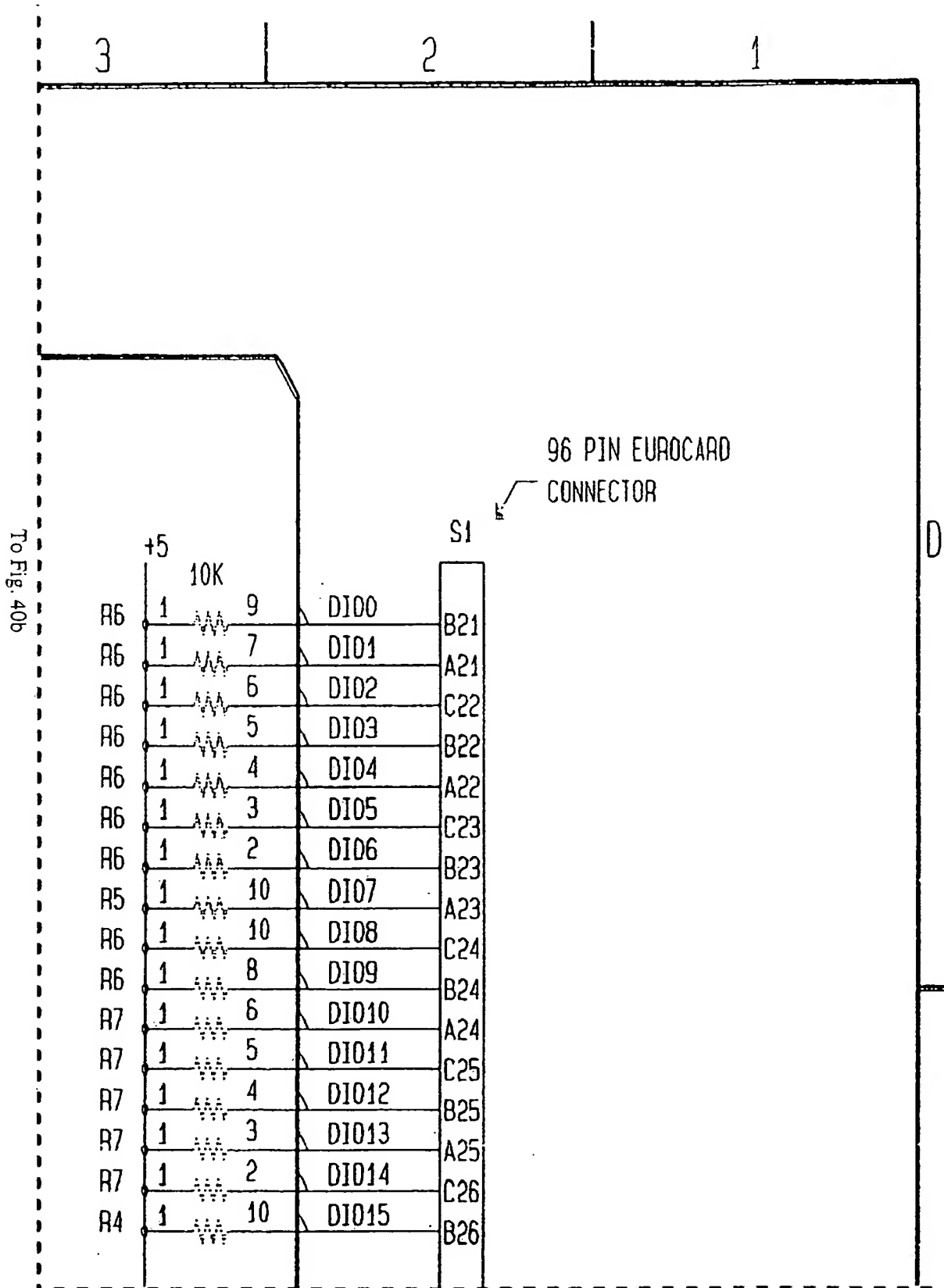
FIG. 39i

145 08 207



146 08207

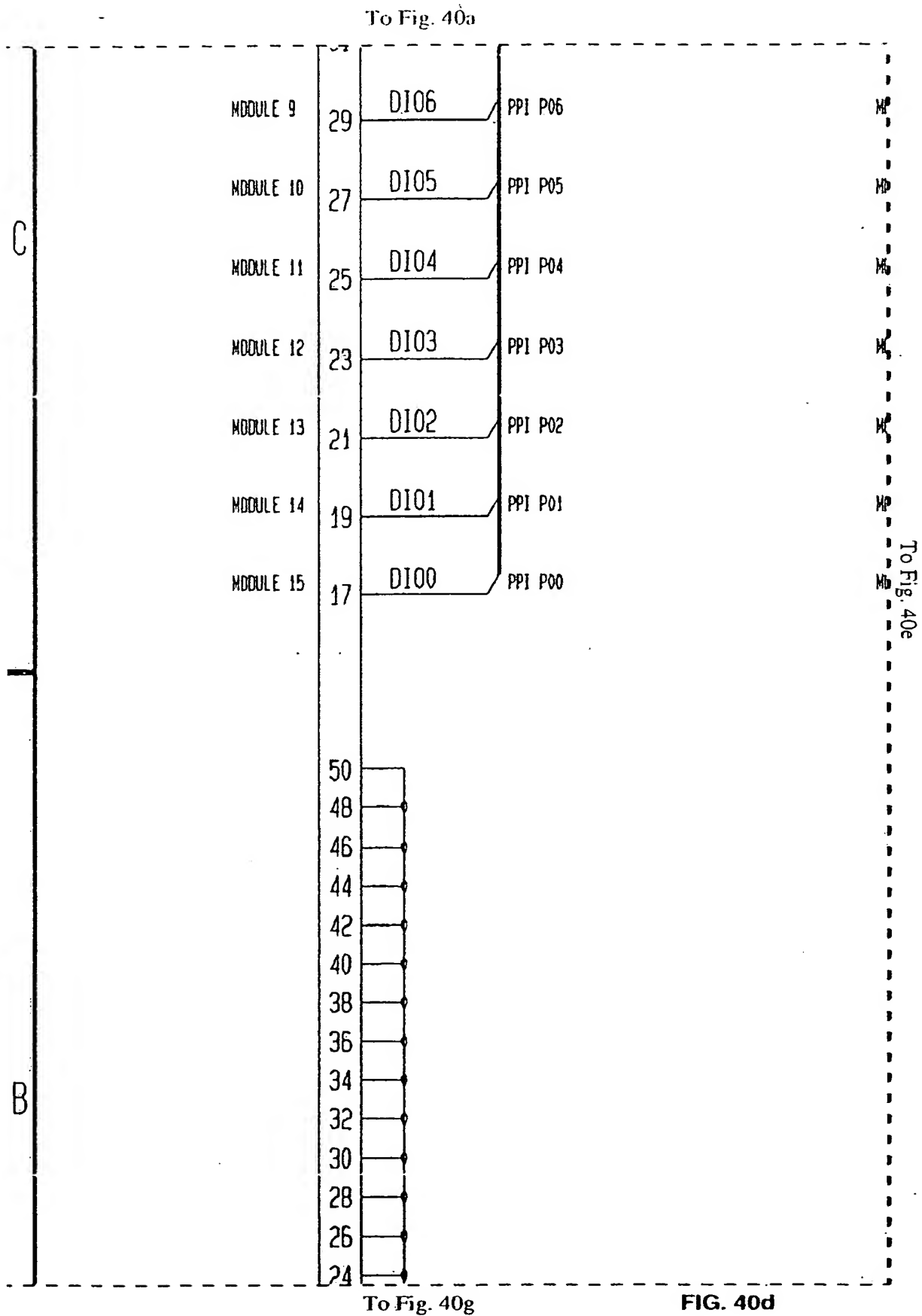




To Fig. 40f

FIG. 40c

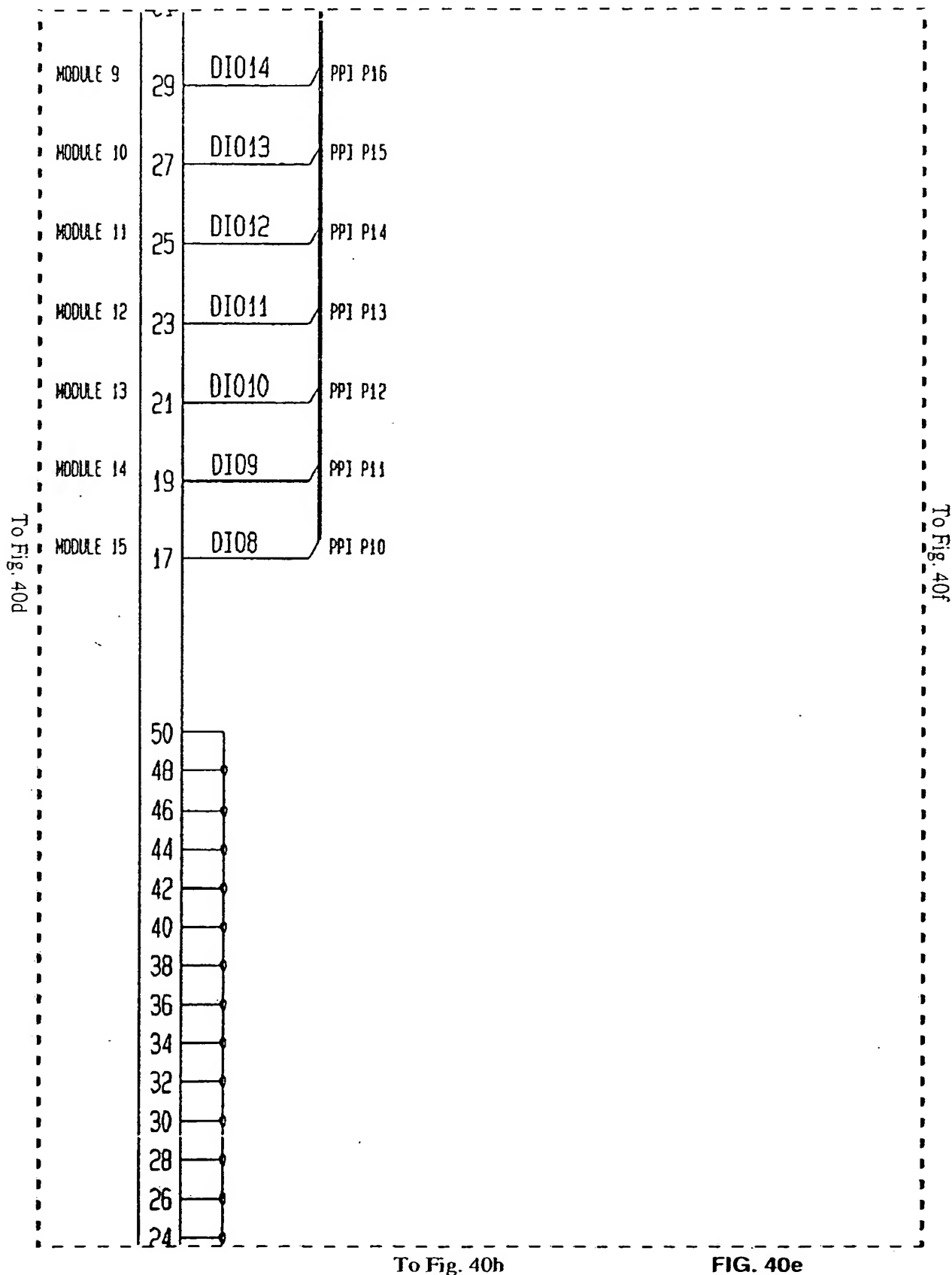
148 08 207





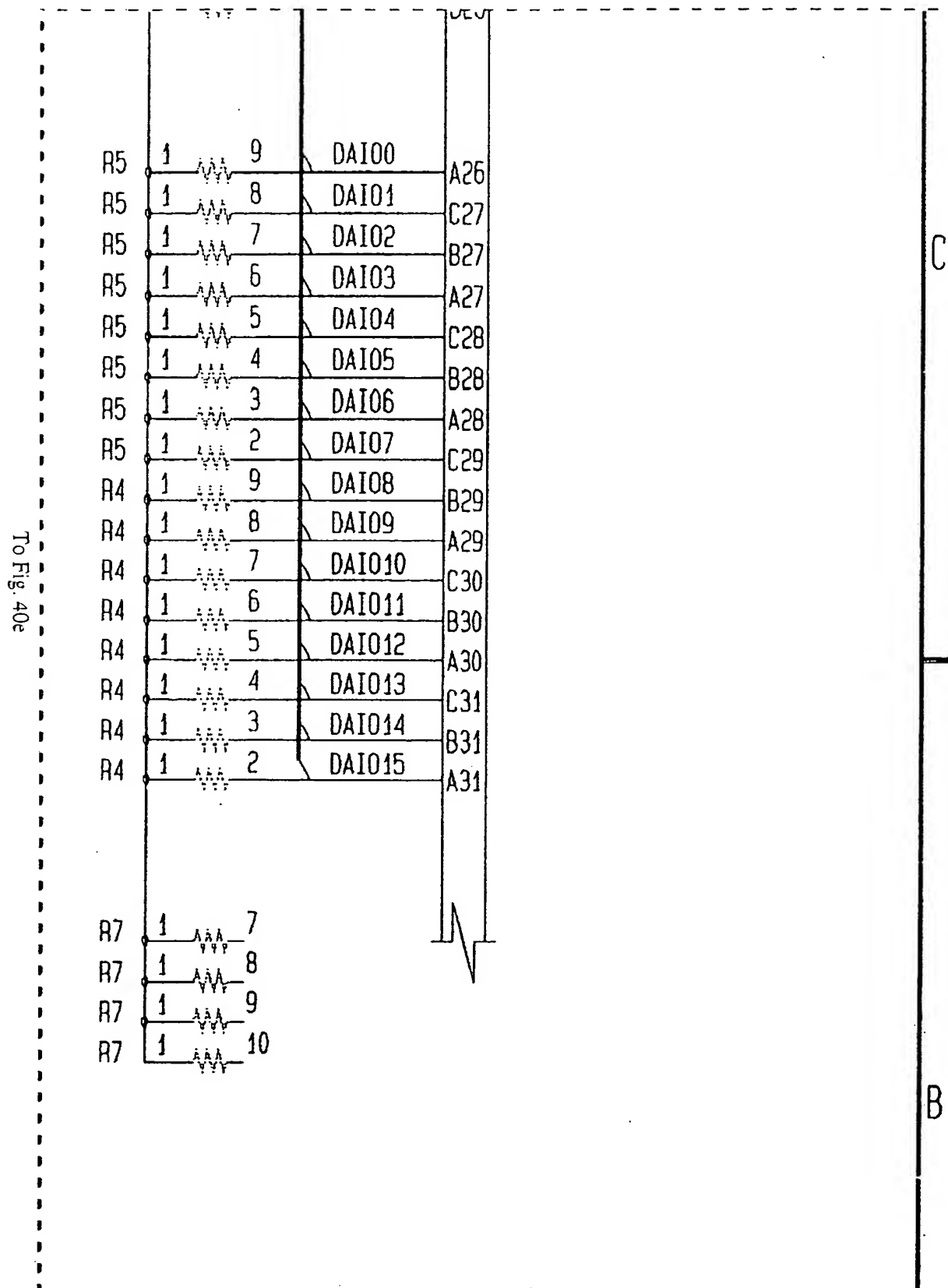
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To Fig. 40b



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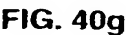
To Fig. 40c



To Fig. 40i

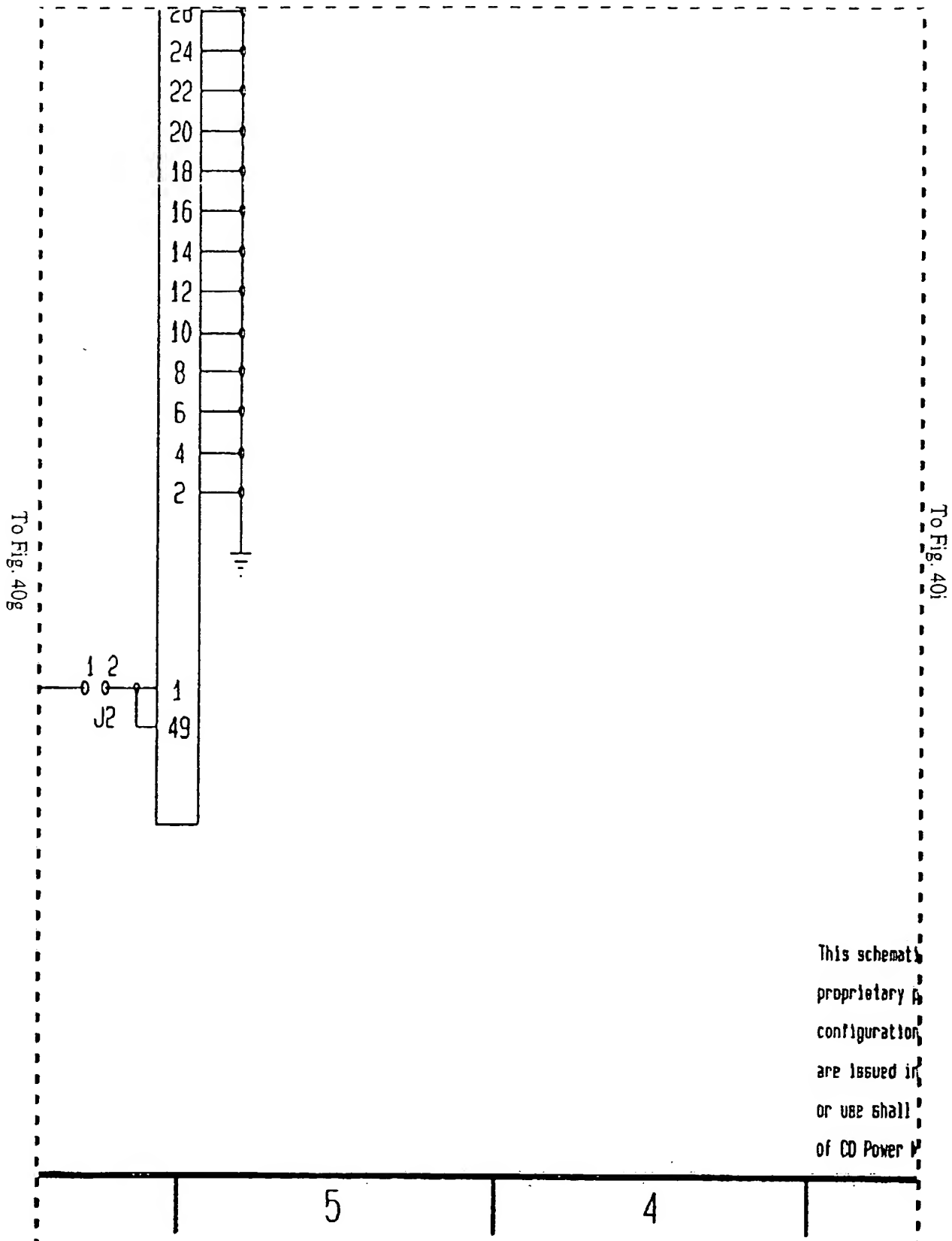
FIG. 40f

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To Fig. 40e



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FIG. 40h

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To Fig. 40f

To Fig. 40h

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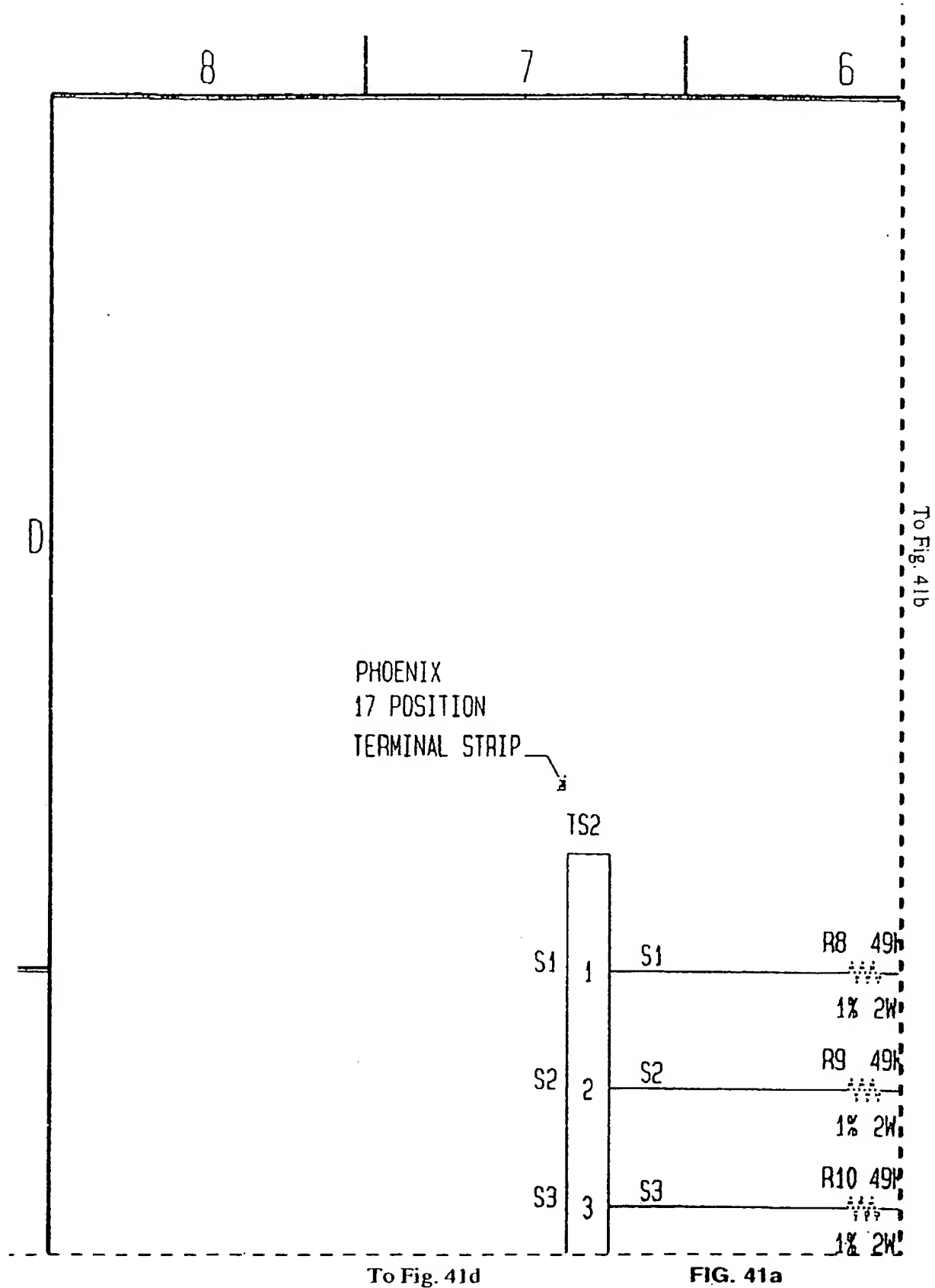
3

2

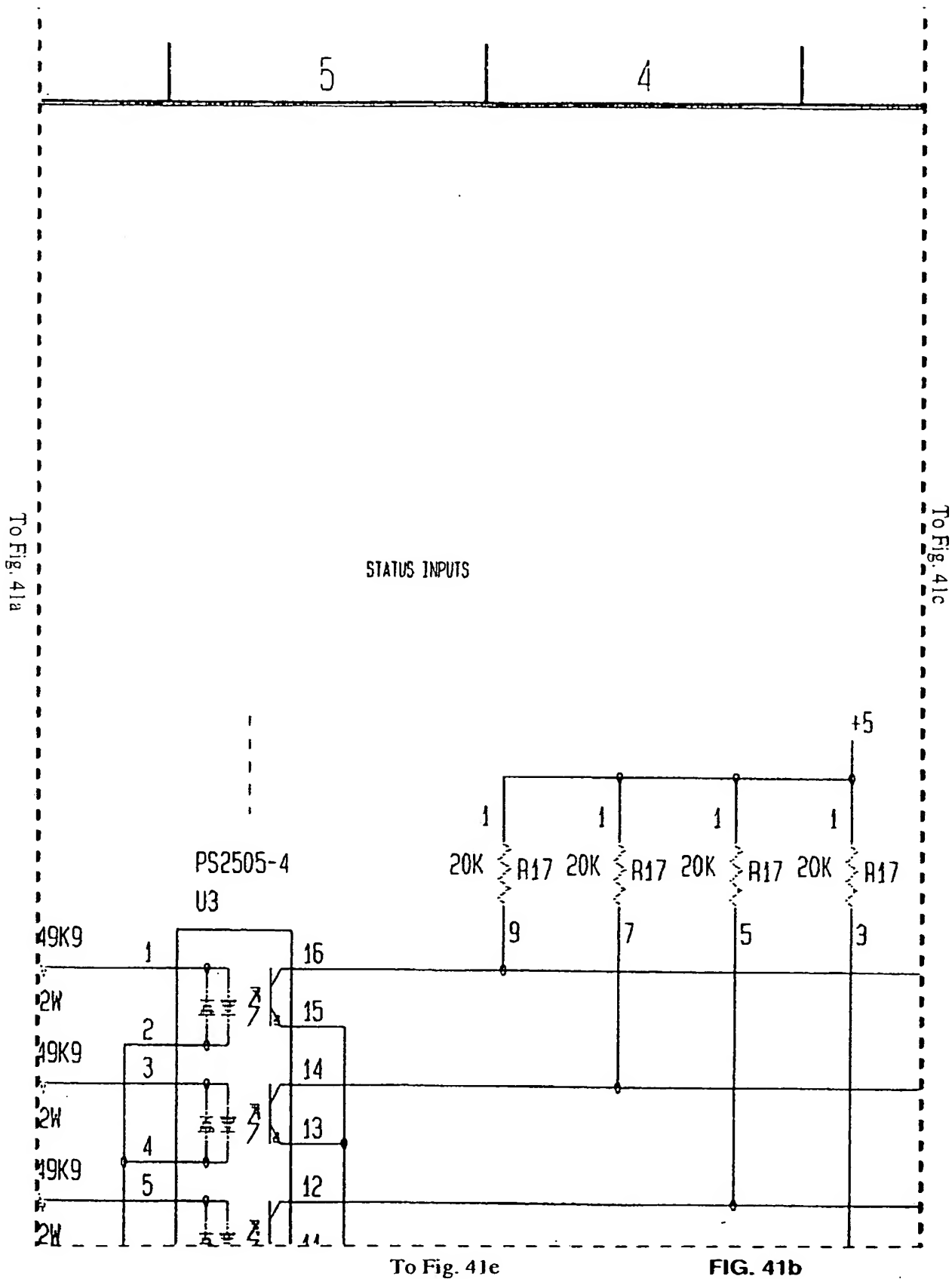
1

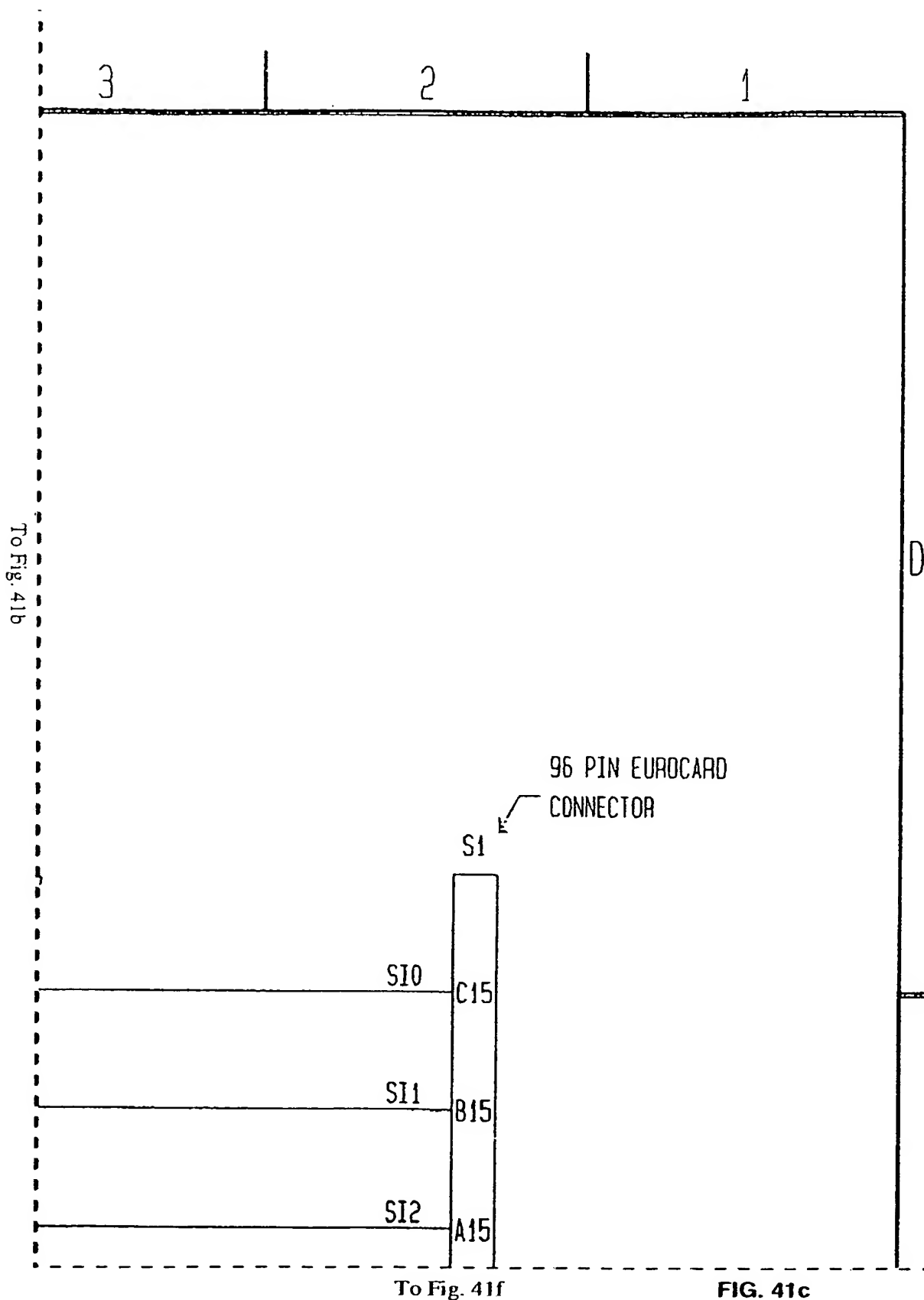
FIG. 40i

154 8 207



155 0207

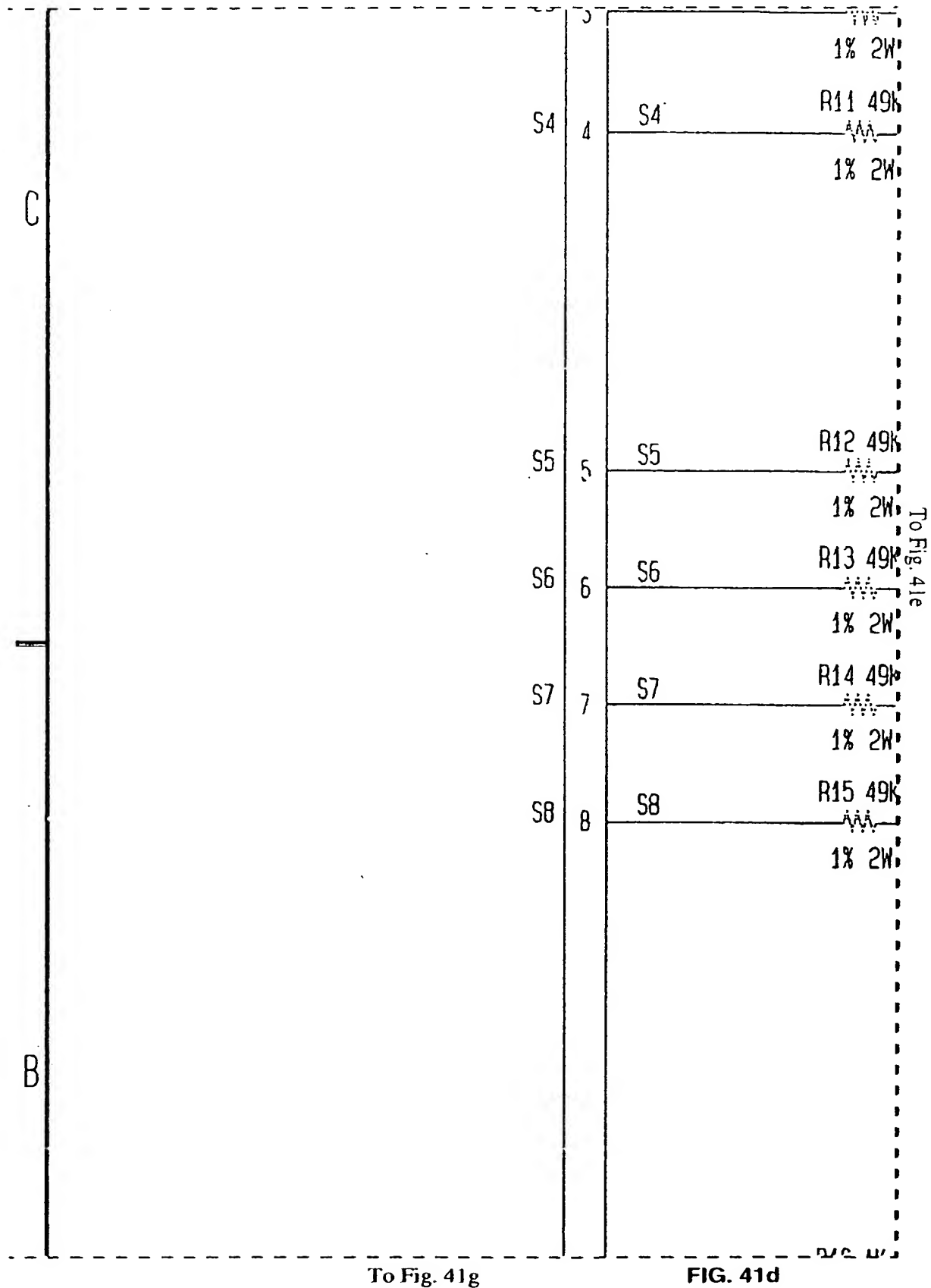






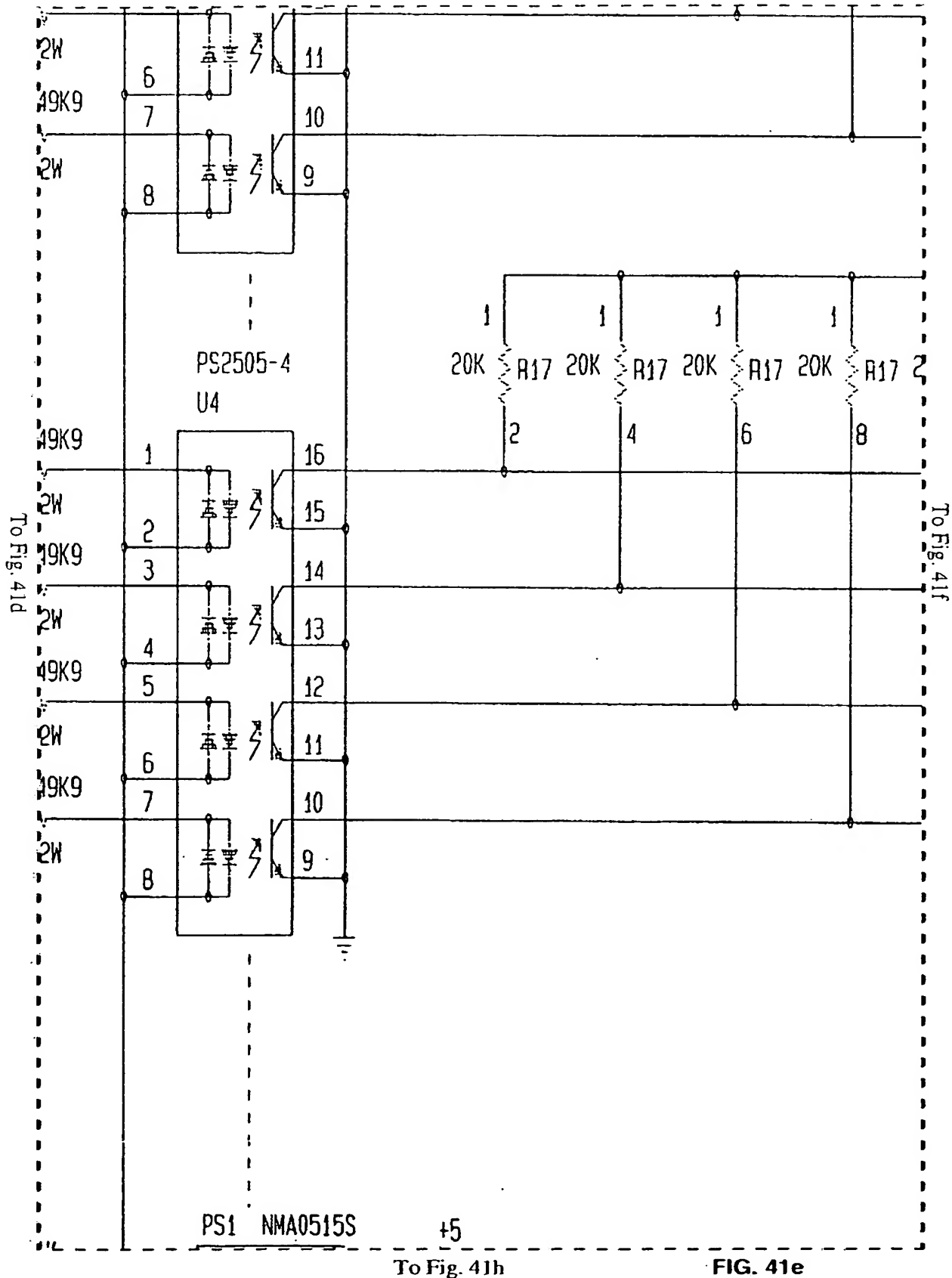
157 08 207

To Fig. 41a



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To Fig. 41b



To Fig. 41h

FIG. 41e

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To Fig. 41c

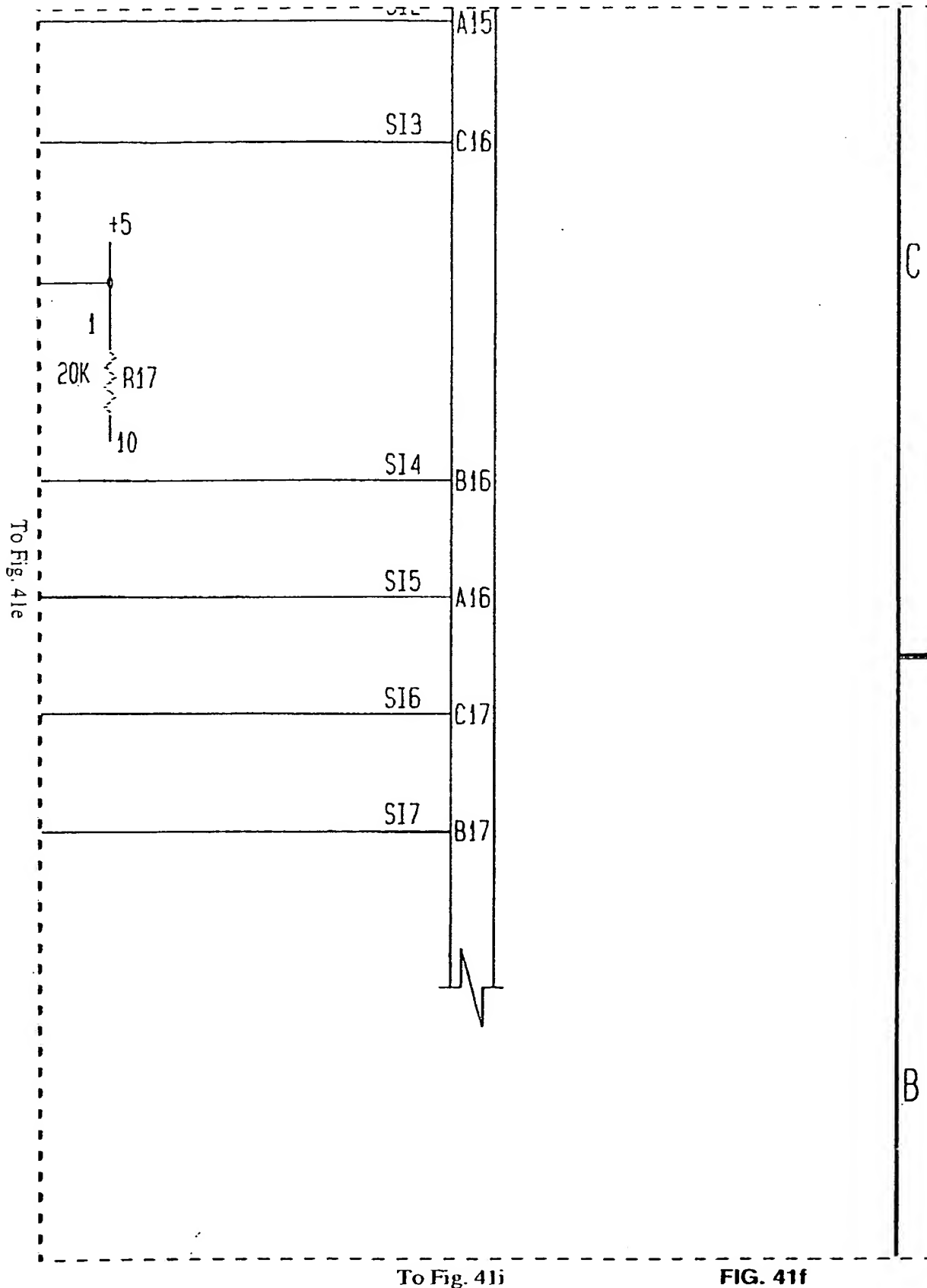
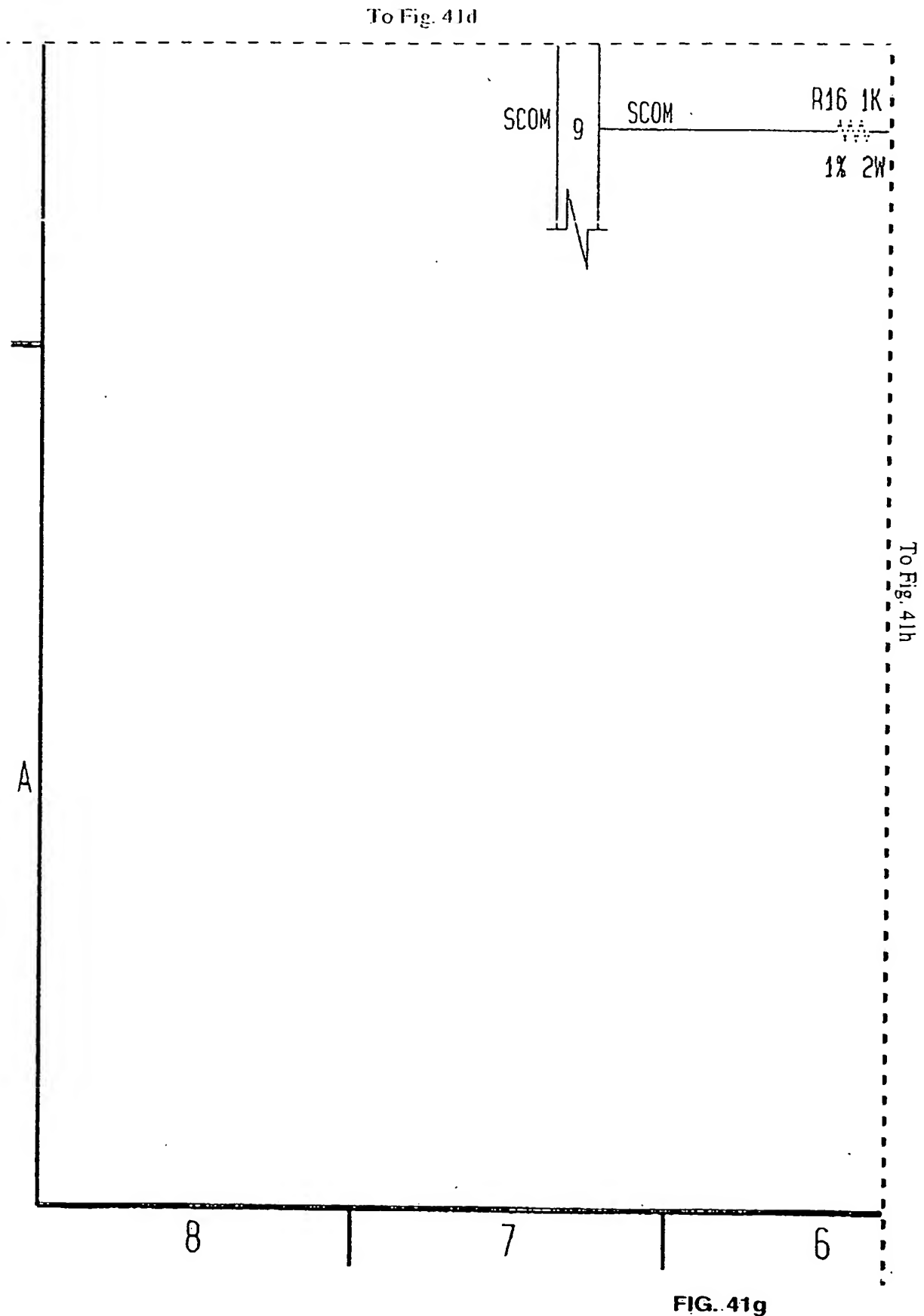


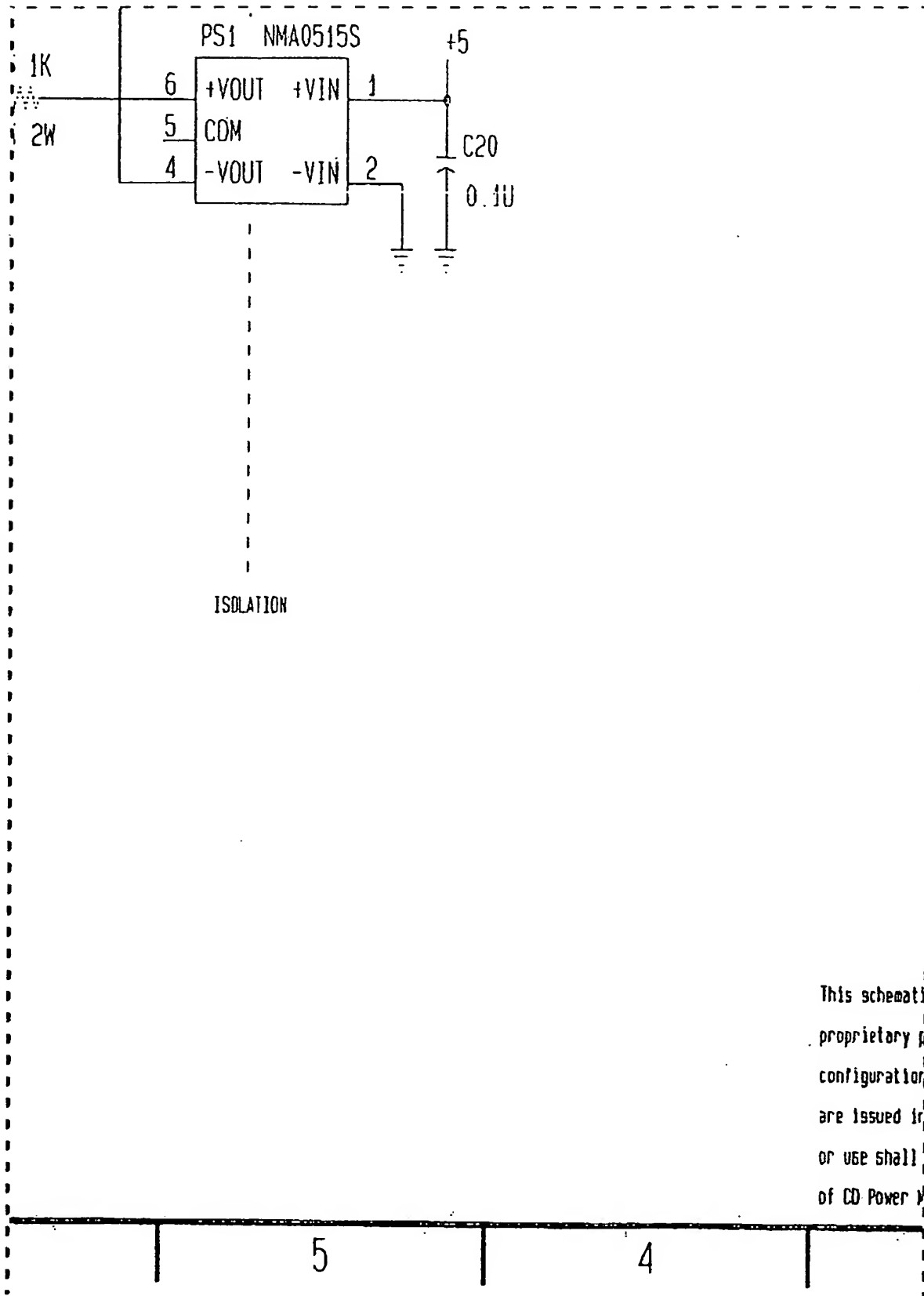
FIG. 41f

160 08 207



161 00307

To Fig. 41c



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FIG. 41h

162 88 007

To Fig. 41f

To Fig. 41h

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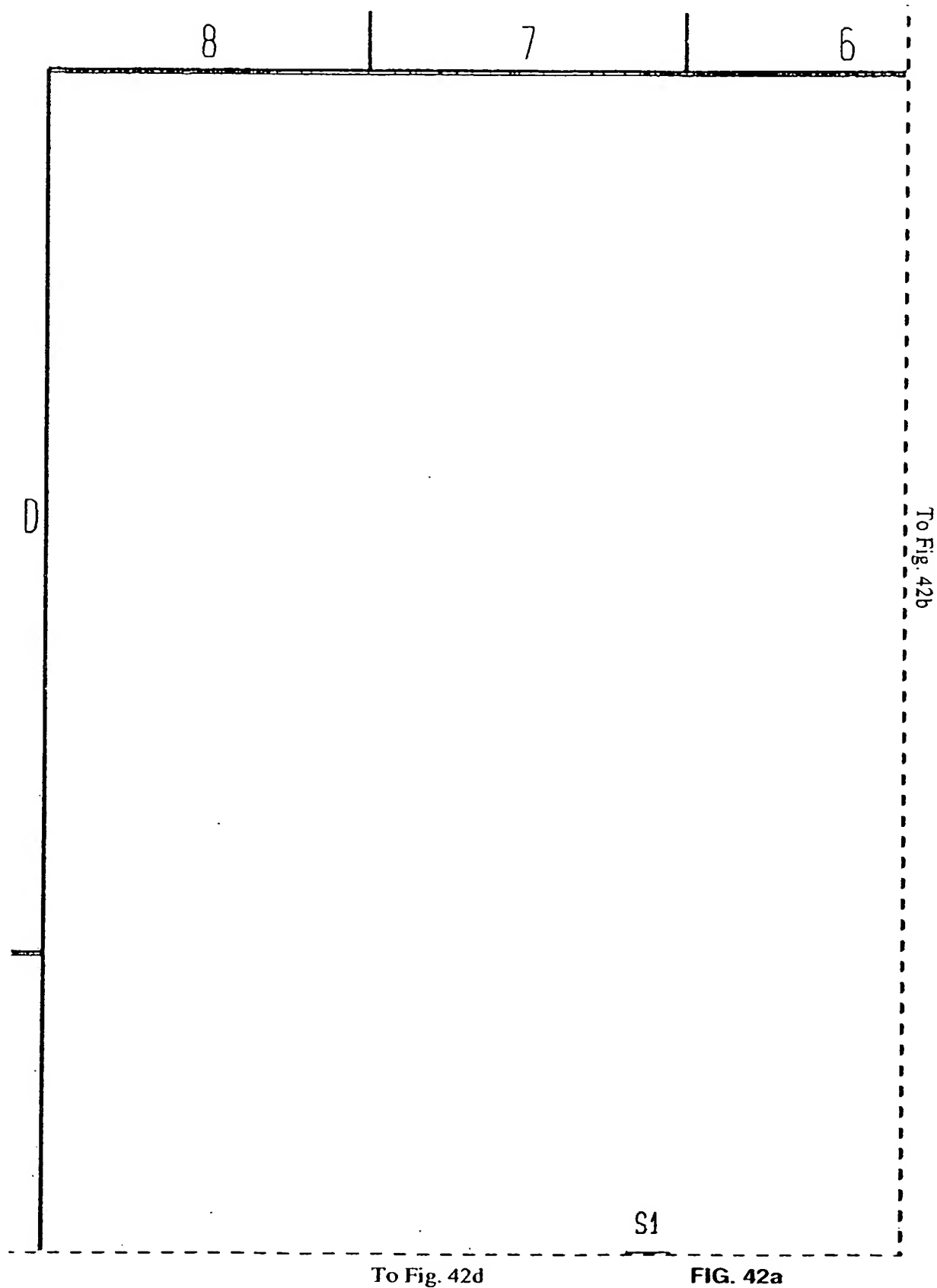
3

2

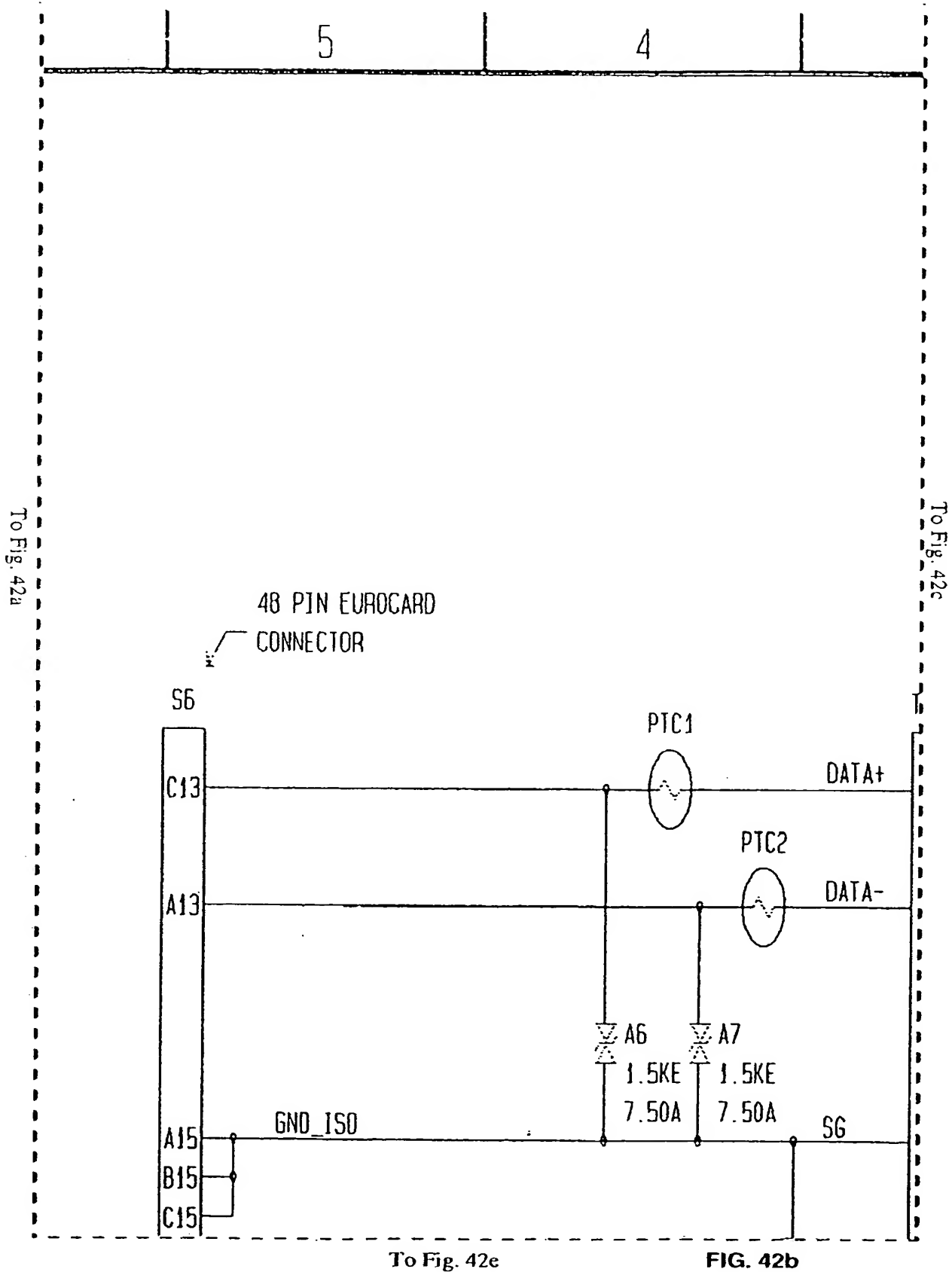
1

FIG. 41i

163 8807

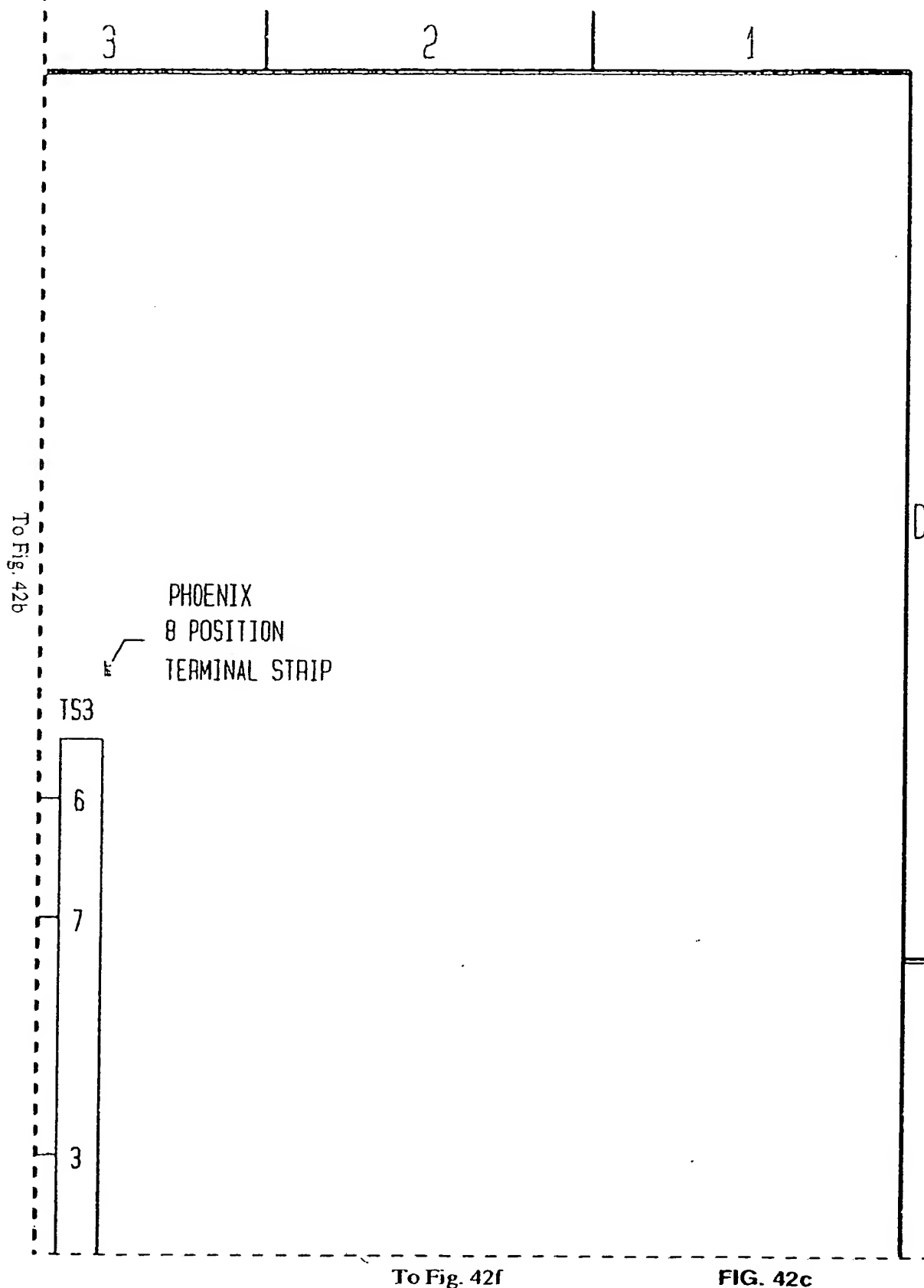


164 58207



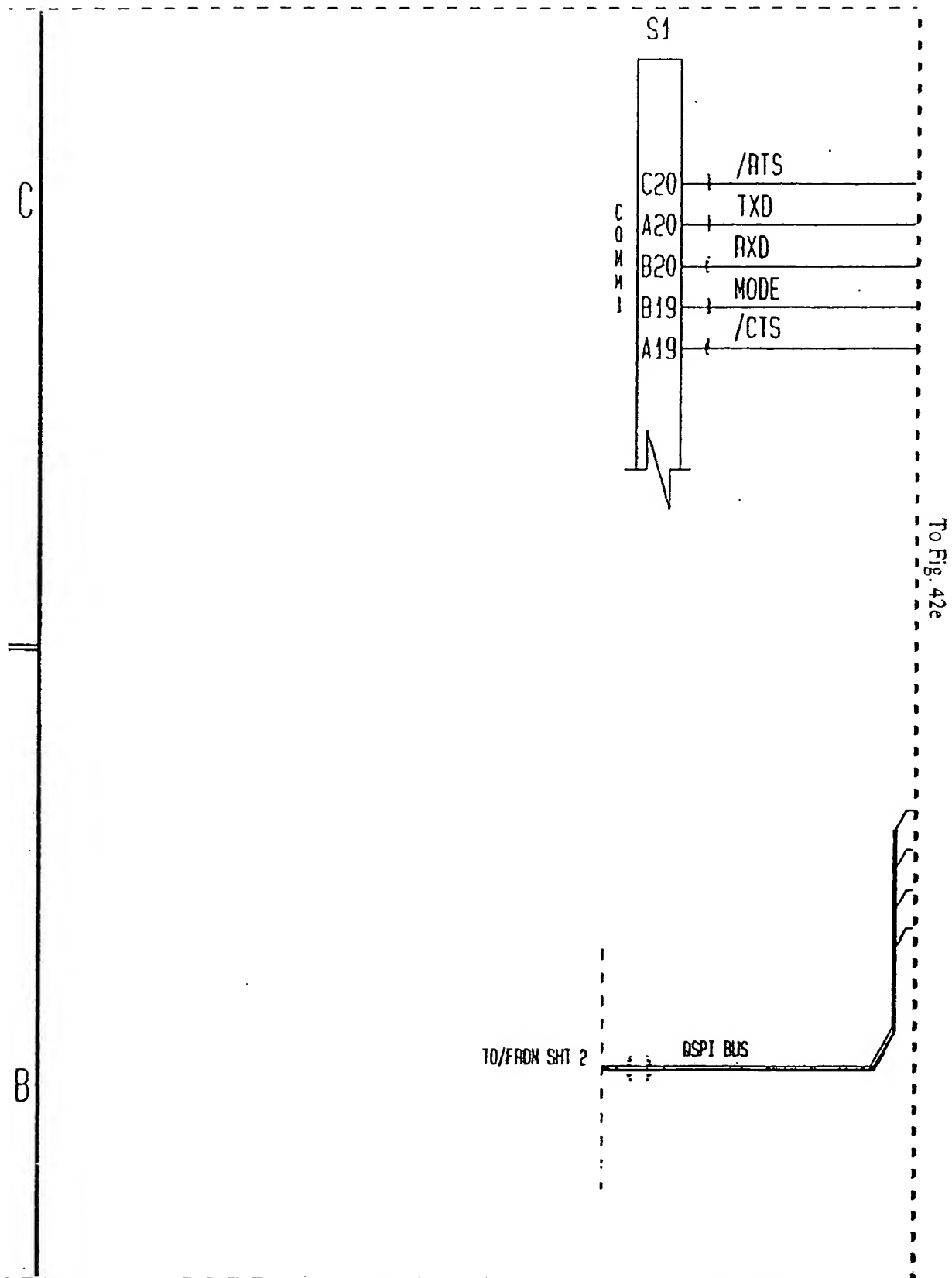


165 17 207



166 00 07

To Fig. 42a

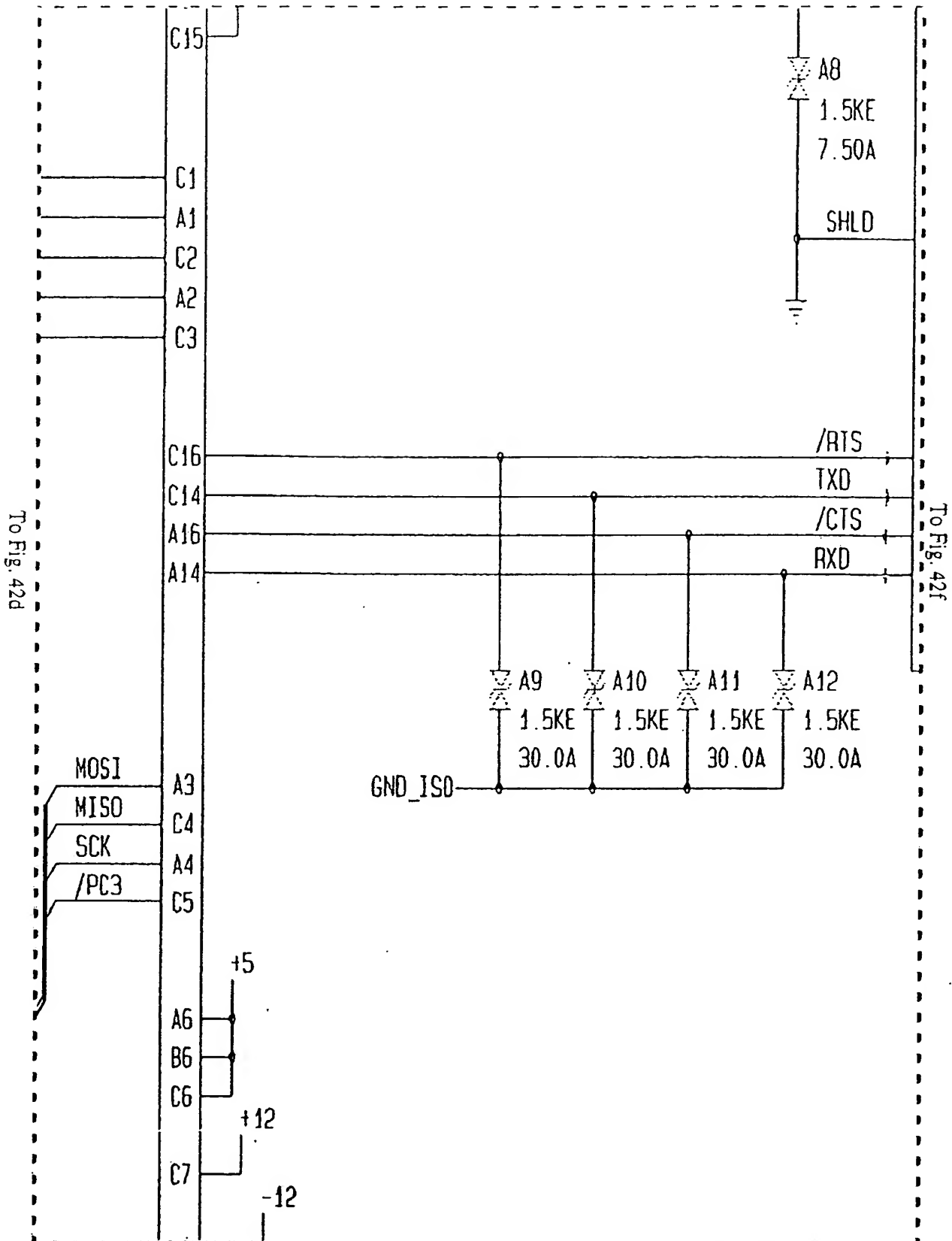


To Fig. 42g

FIG. 42d

167 07 207

To Fig. 42b

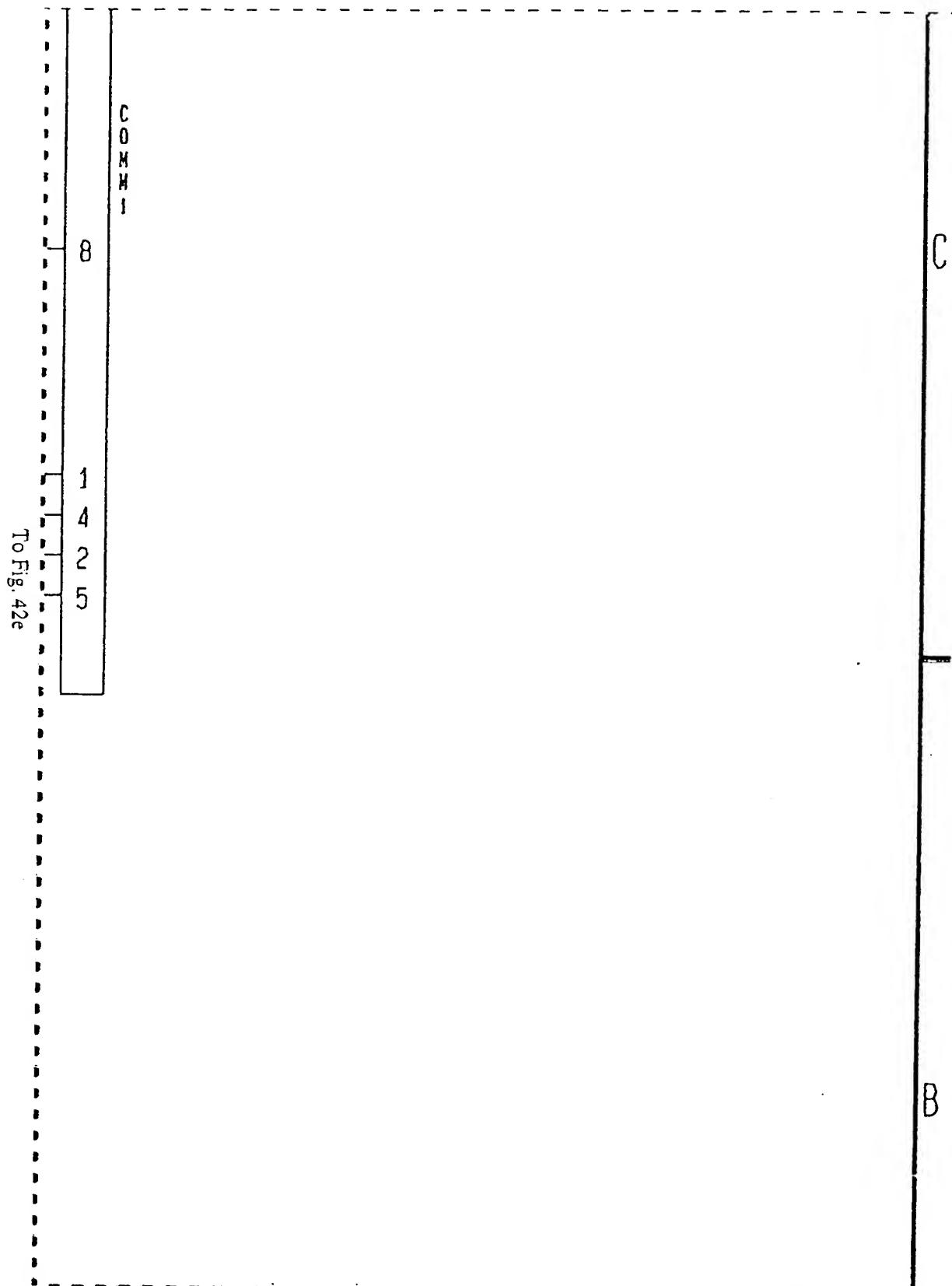


To Fig. 42h

FIG. 42e

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To Fig. 42c



To Fig. 42d

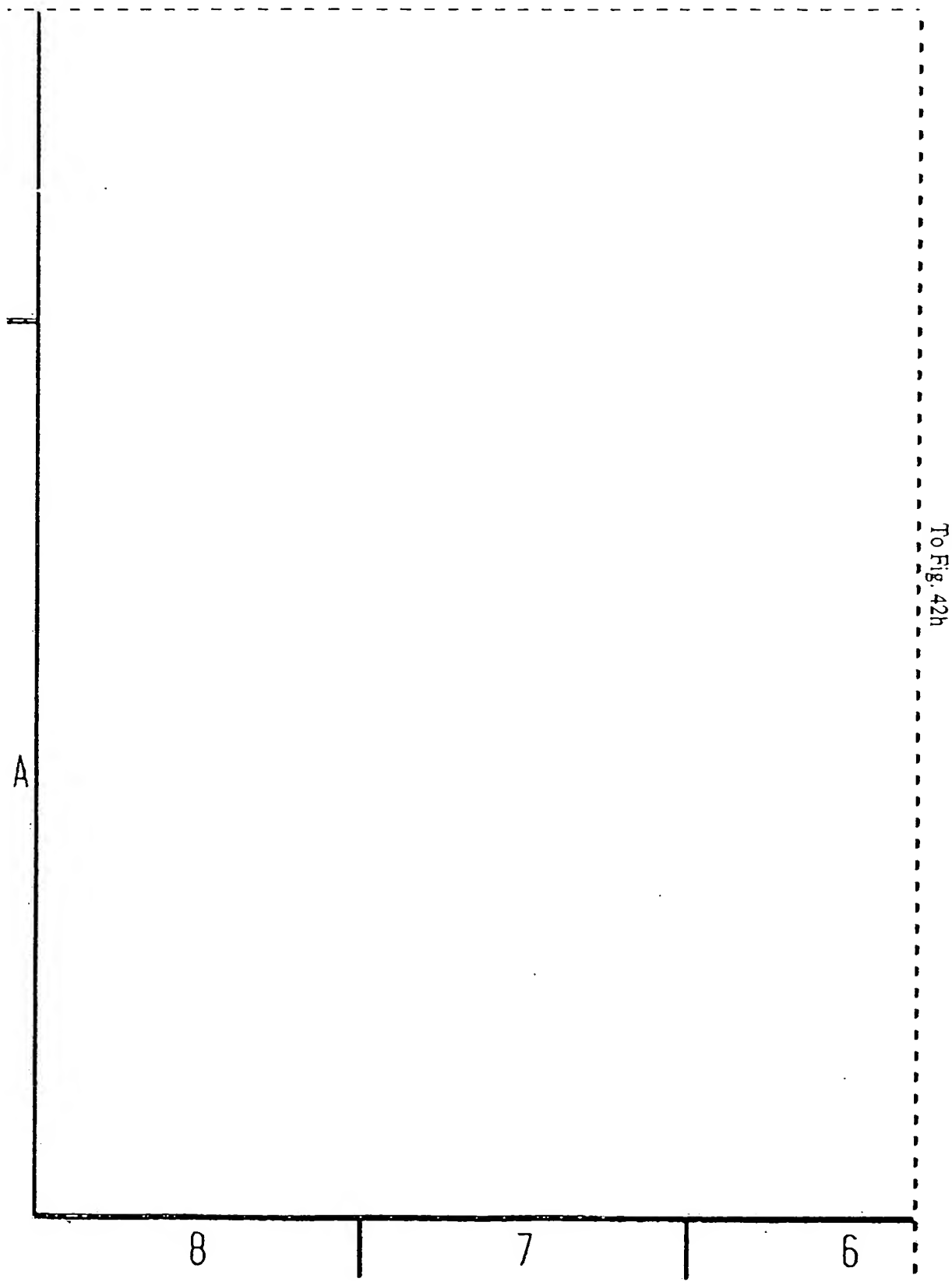
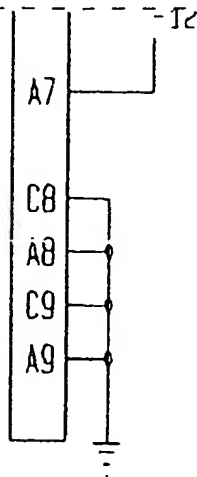


FIG. 42g

To Fig. 42e



To Fig. 42g

To Fig. 42i

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5

4


FIG. 42h

171 6207

To Fig. 42f

To Fig. 42h

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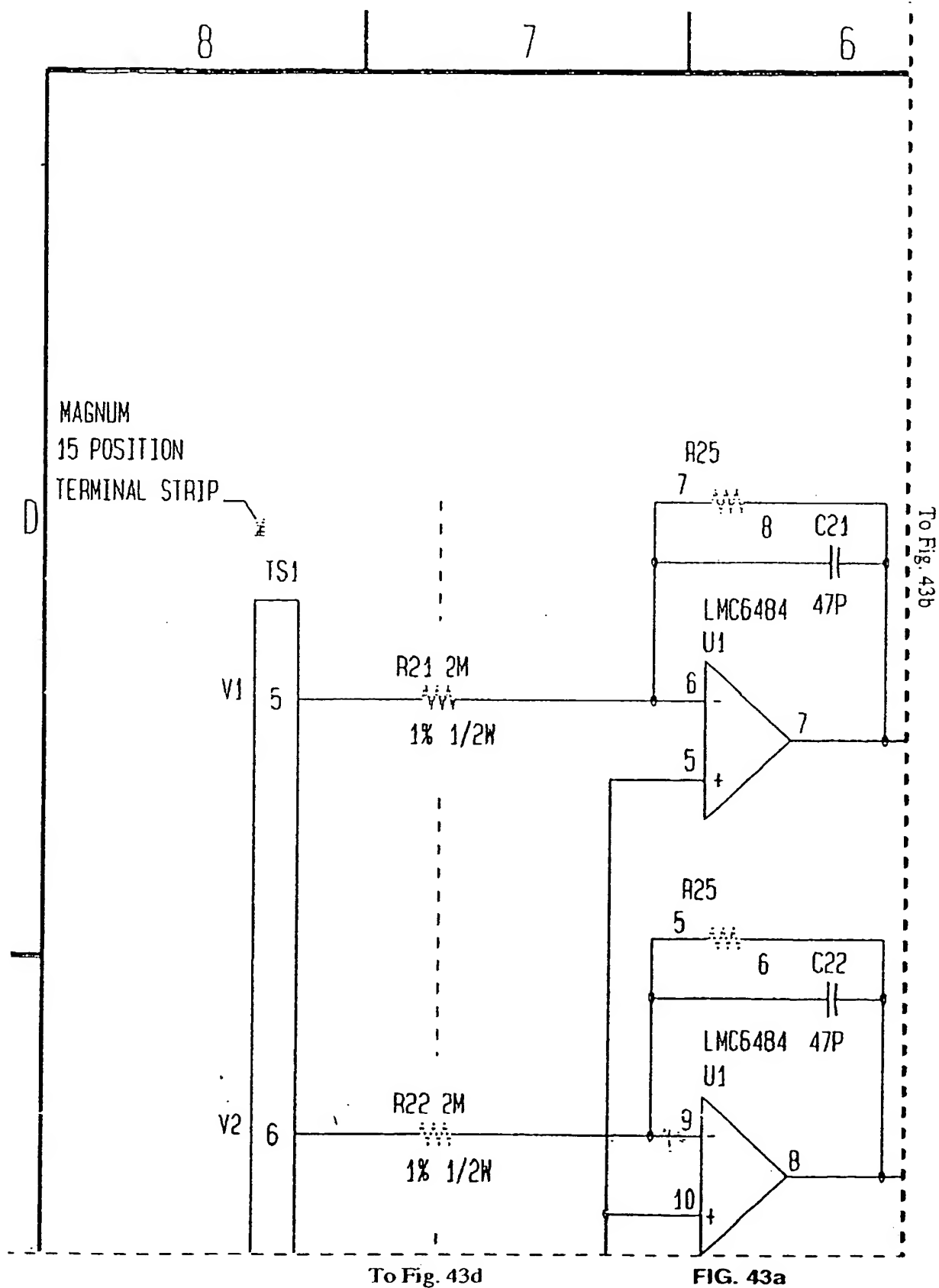
3

2

1

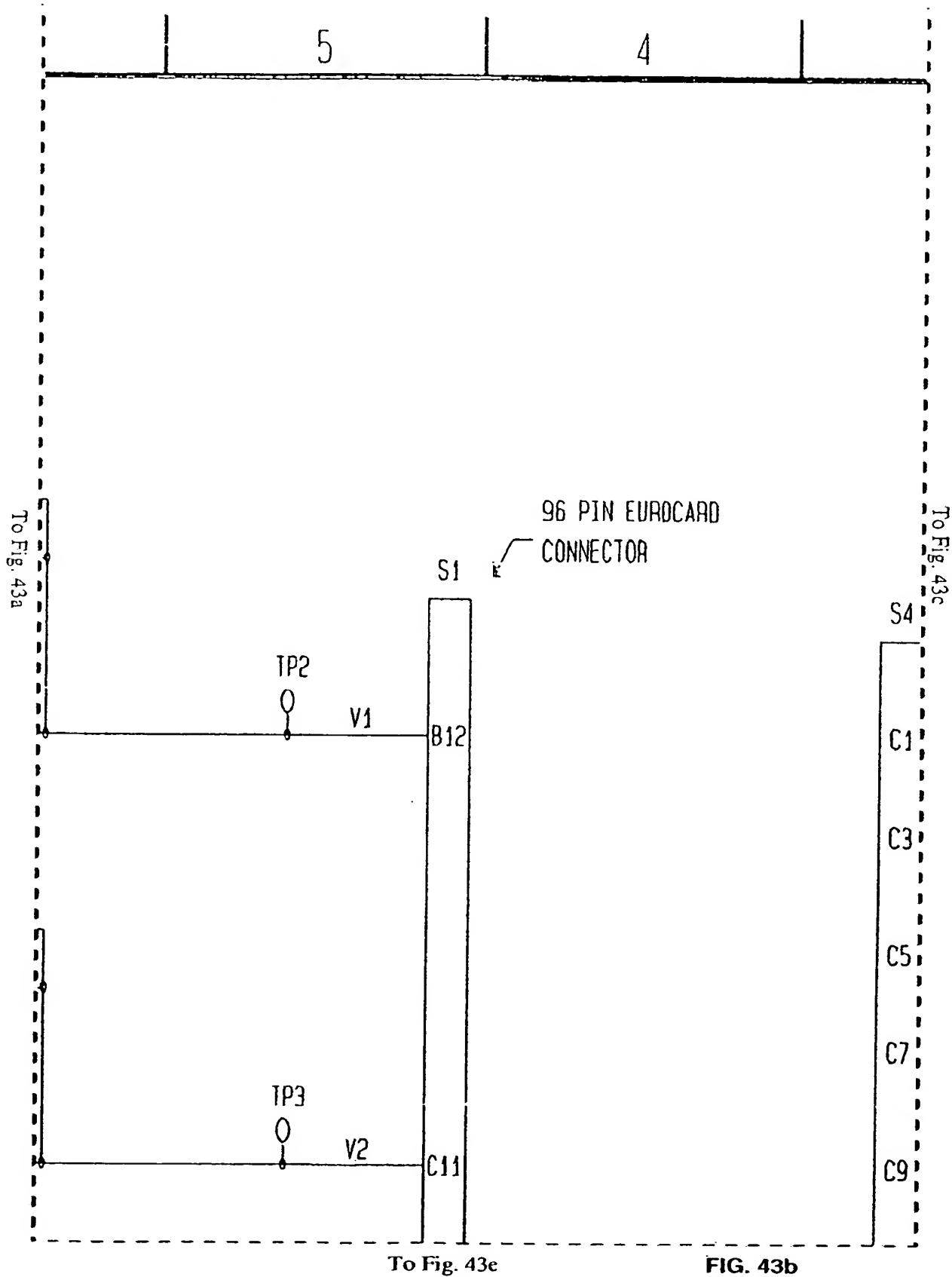
FIG. 42i

172 9807

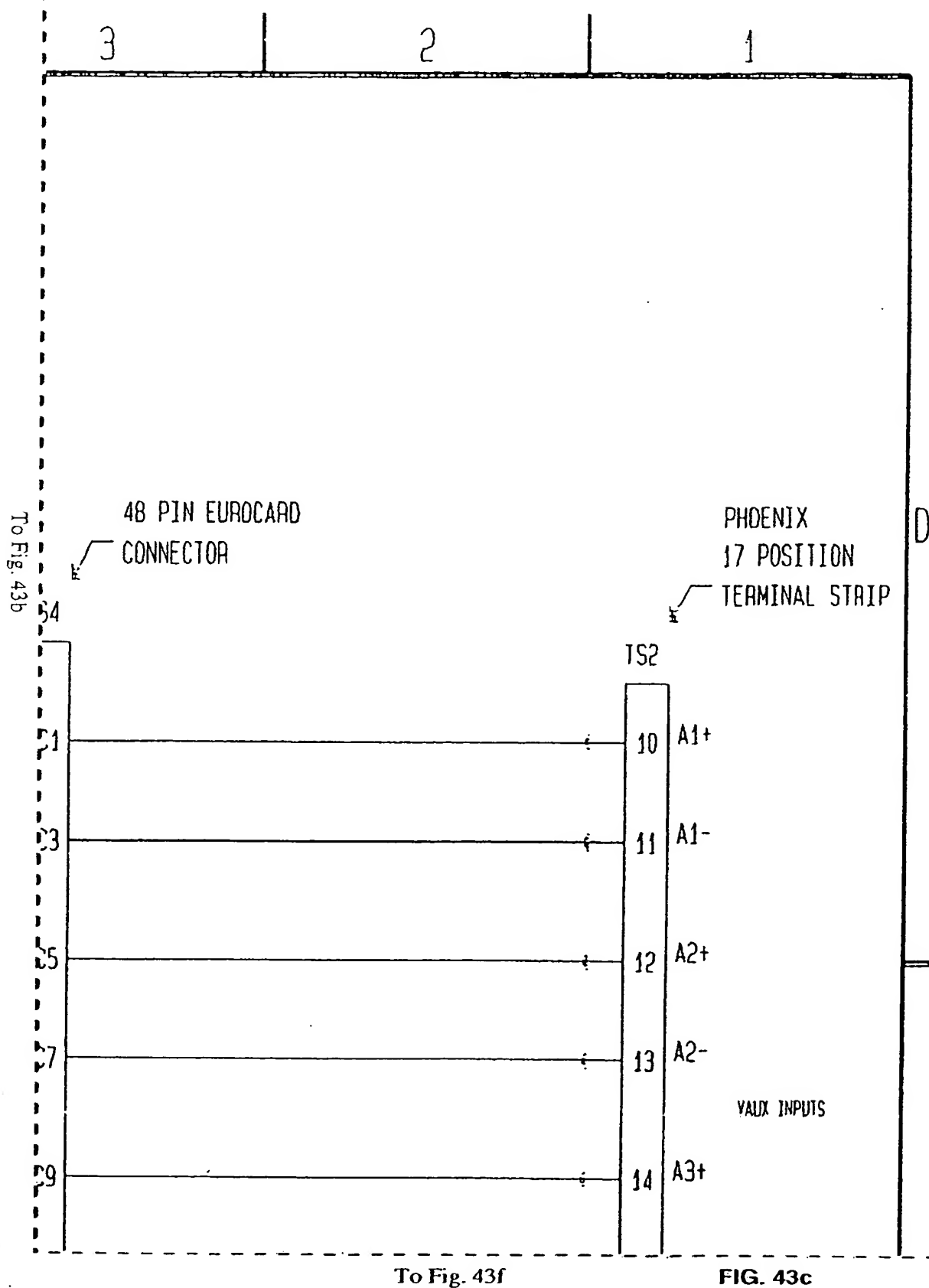




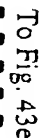
173 8 207



174 06 207



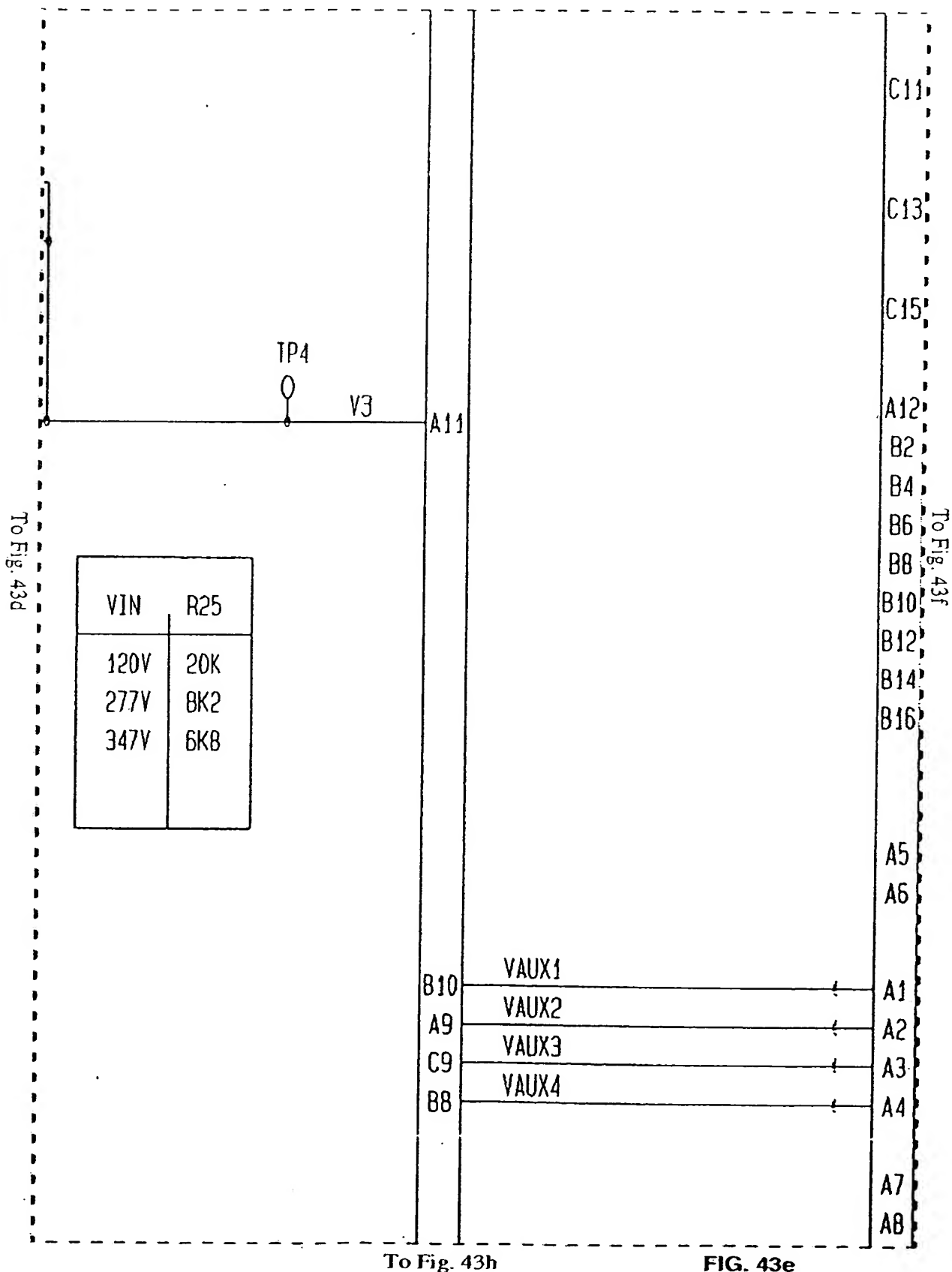
ISOLATION  
2KV



**FIG. 43d**

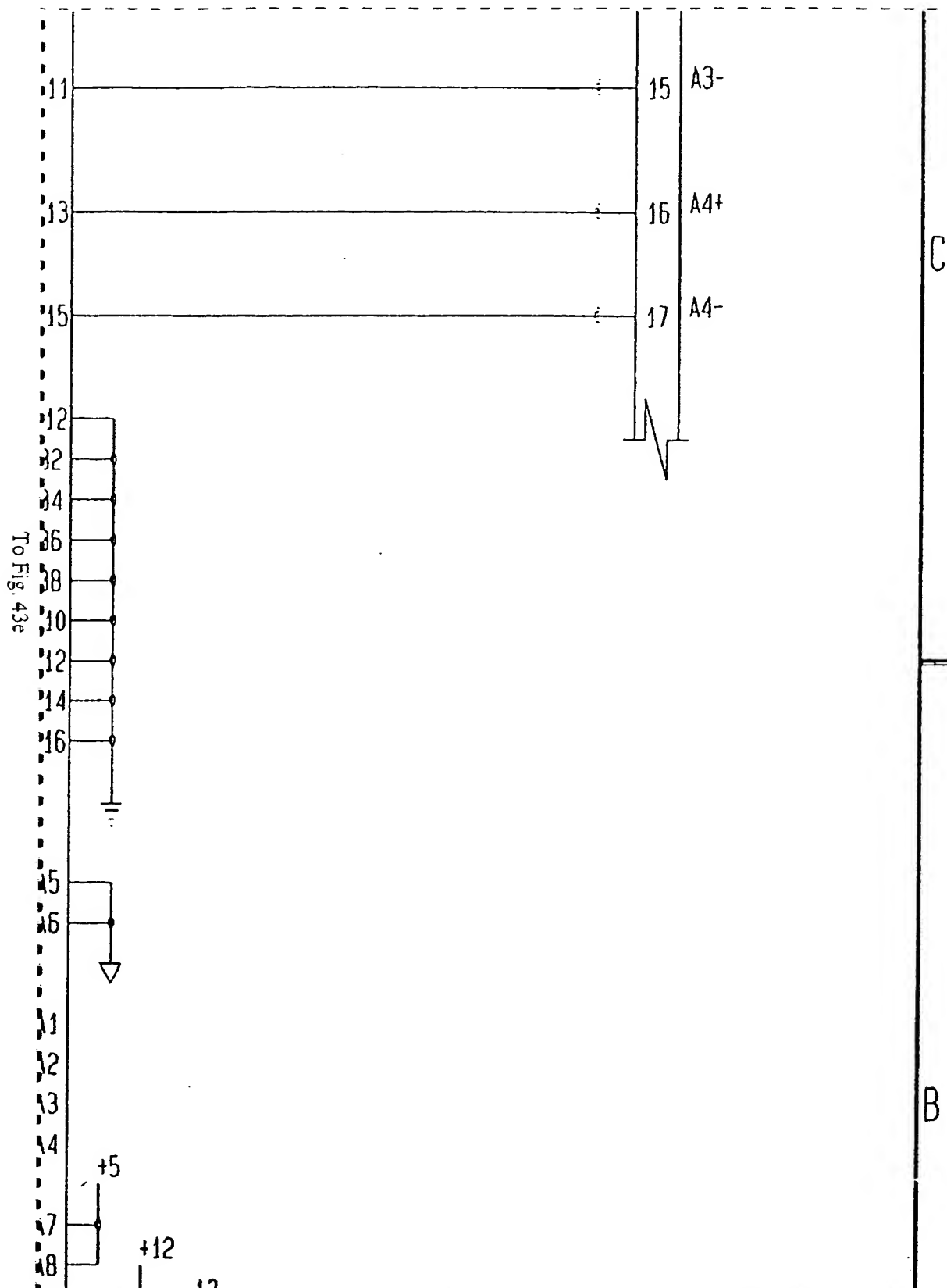
176 08 207

To Fig. 43b



177 ab 207

To Fig. 43c



To Fig. 43i

FIG. 43f

178 06 807

To Fig. 43d

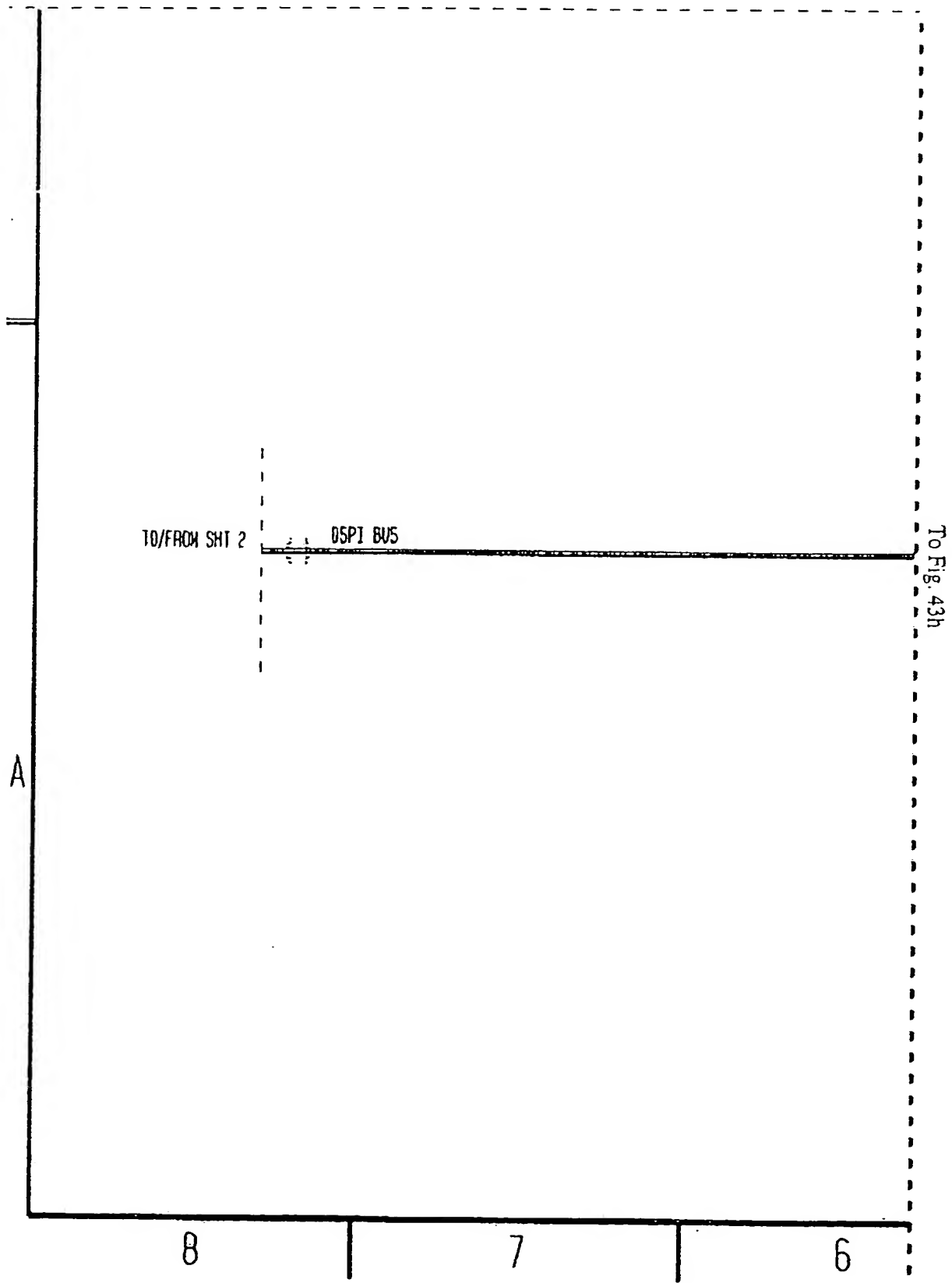
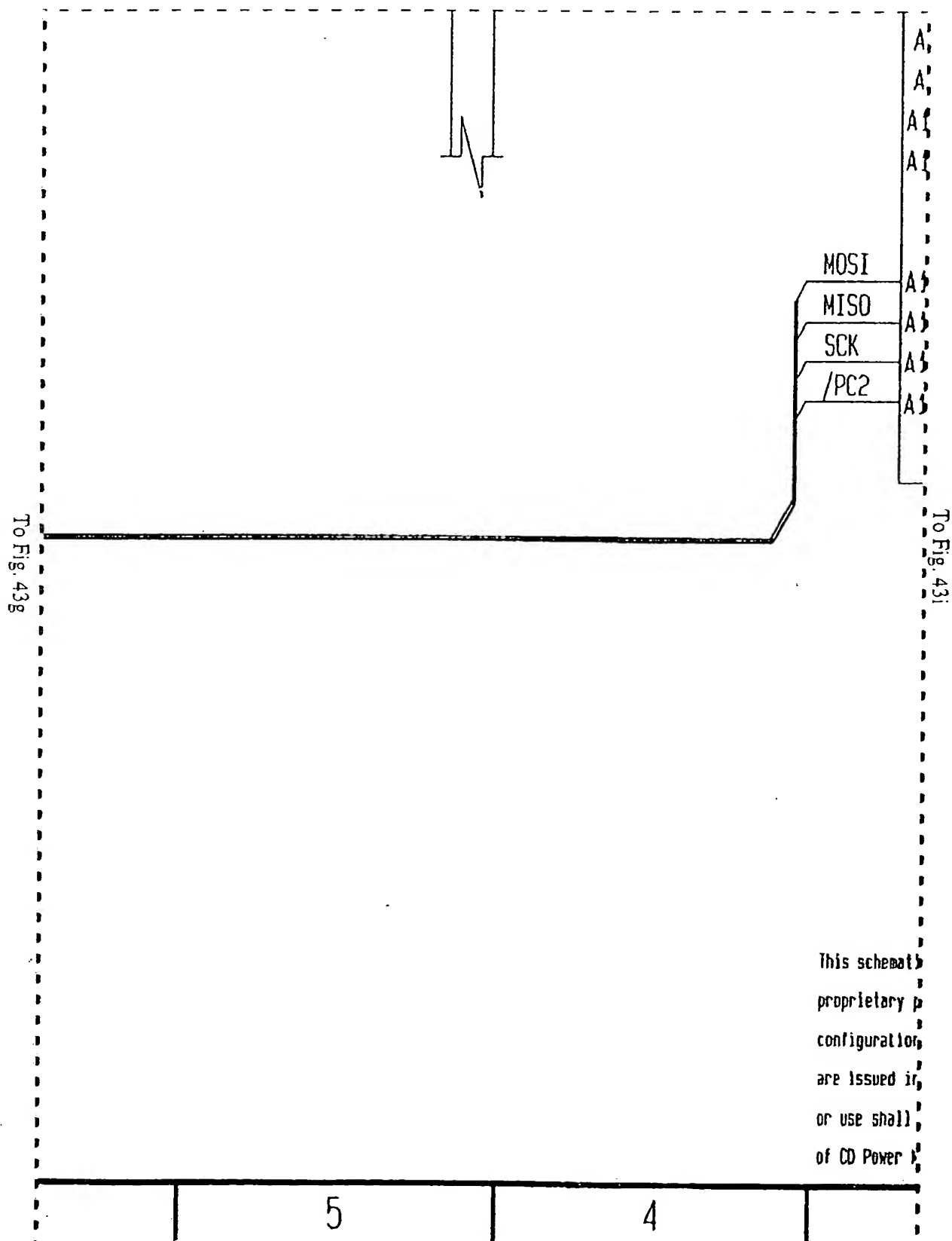


FIG. 43g

179 08 207

To Fig. 43e



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FIG. 43h

180 08 207

To Fig. 43f

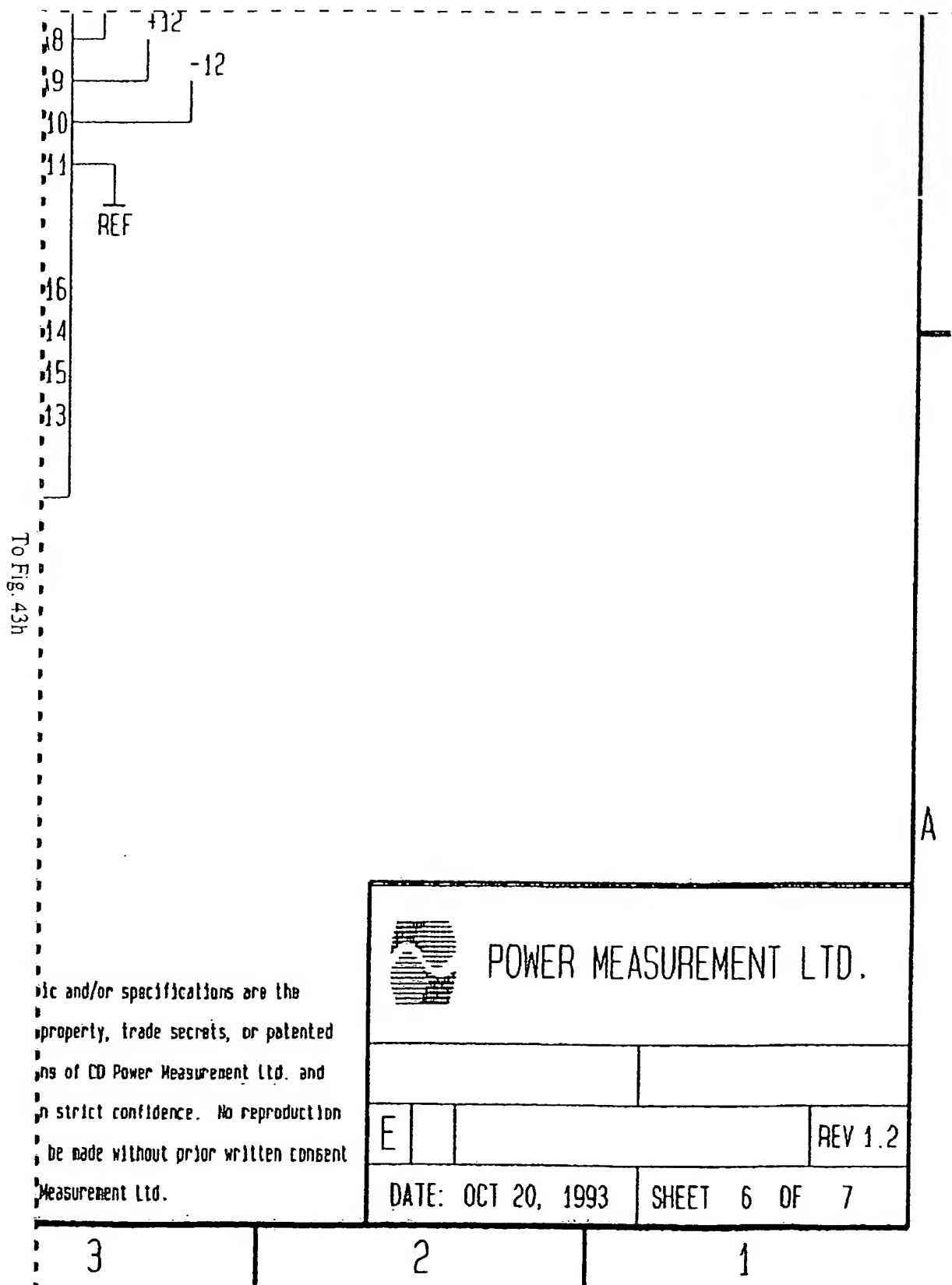
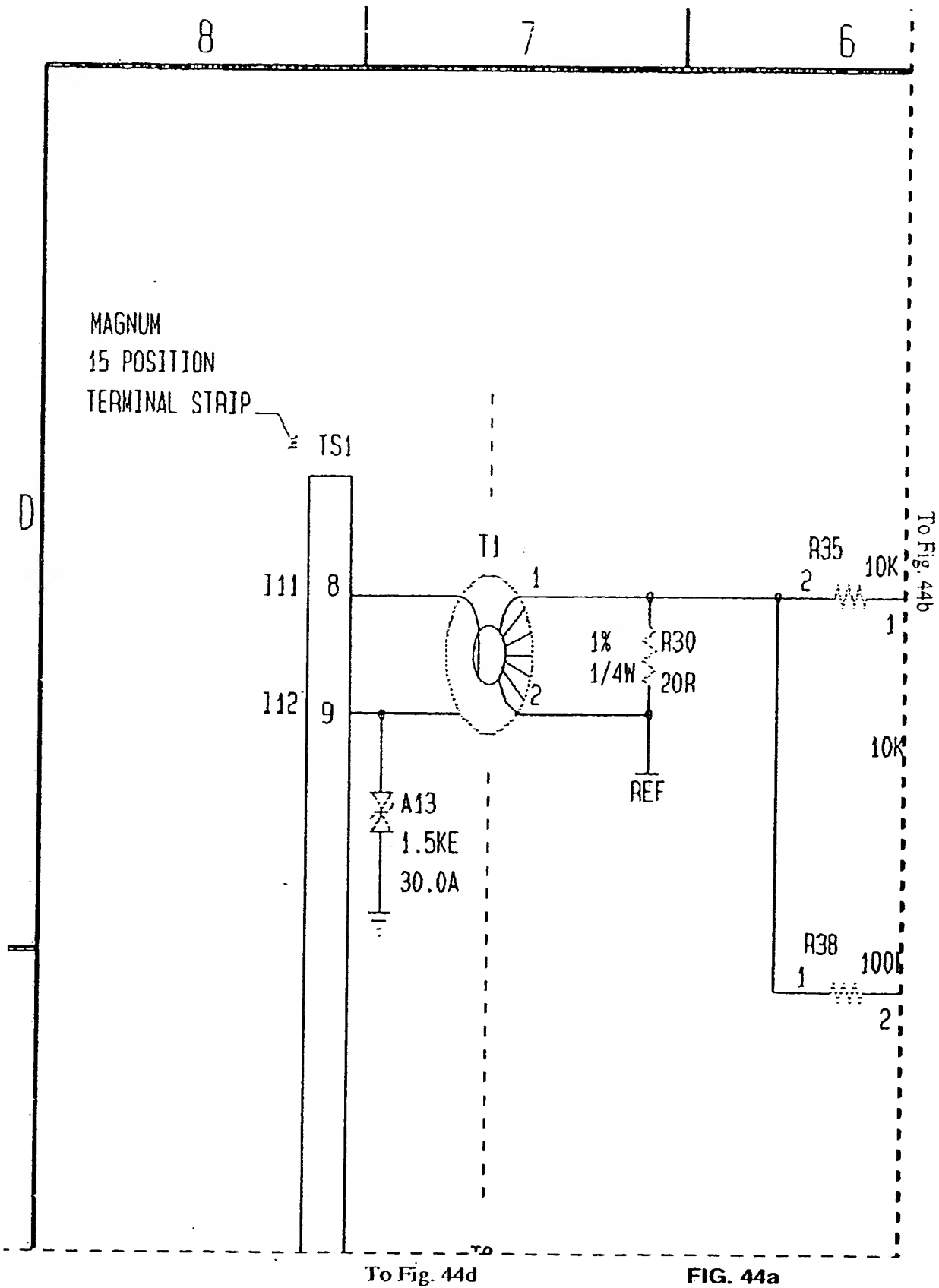


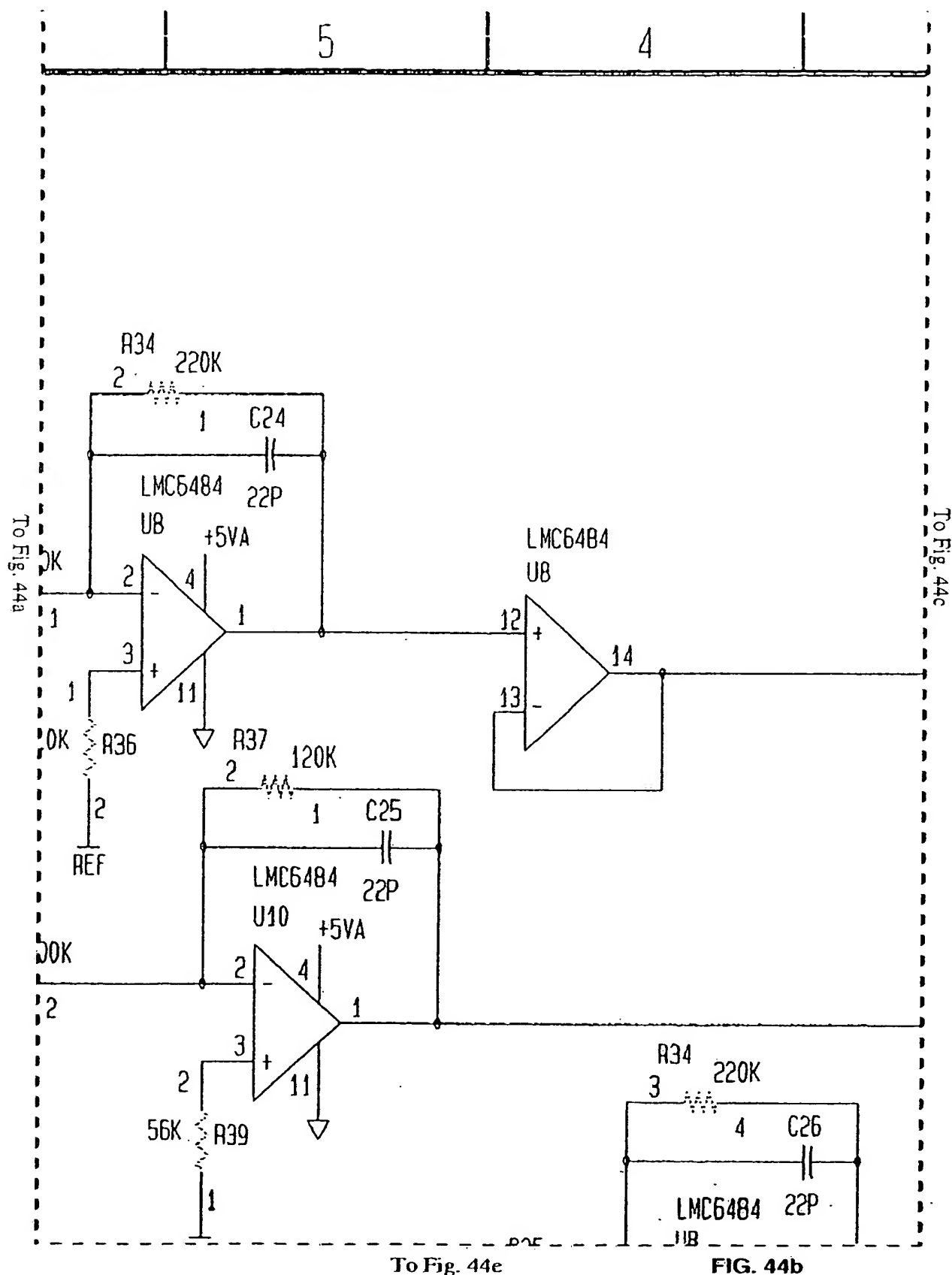
FIG. 43i



181 60 207



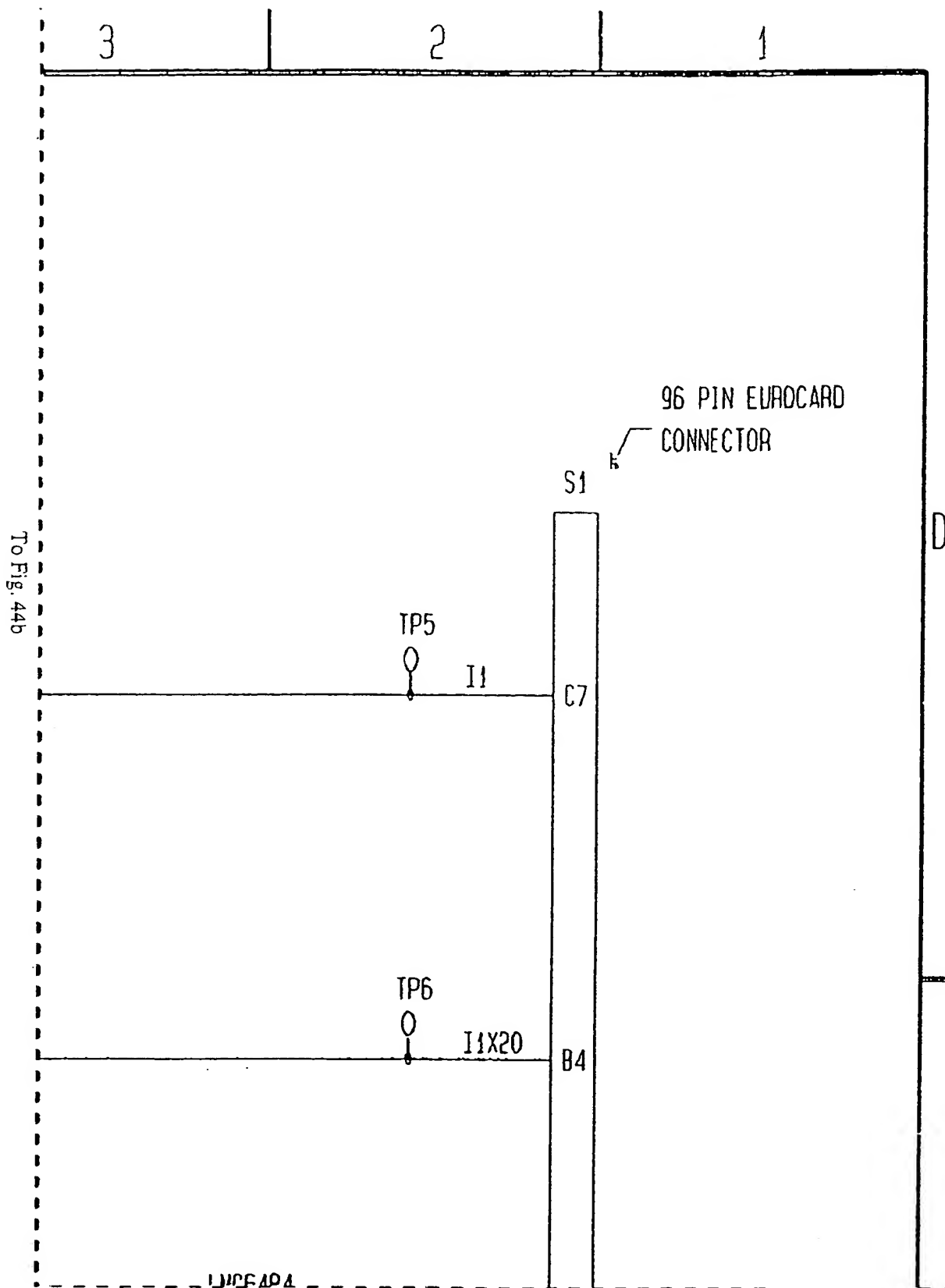
182 06 207



To Fig. 44e

FIG. 44b

183 07 207



To Fig. 44f

FIG. 44c

184 06 207

To Fig. 44a

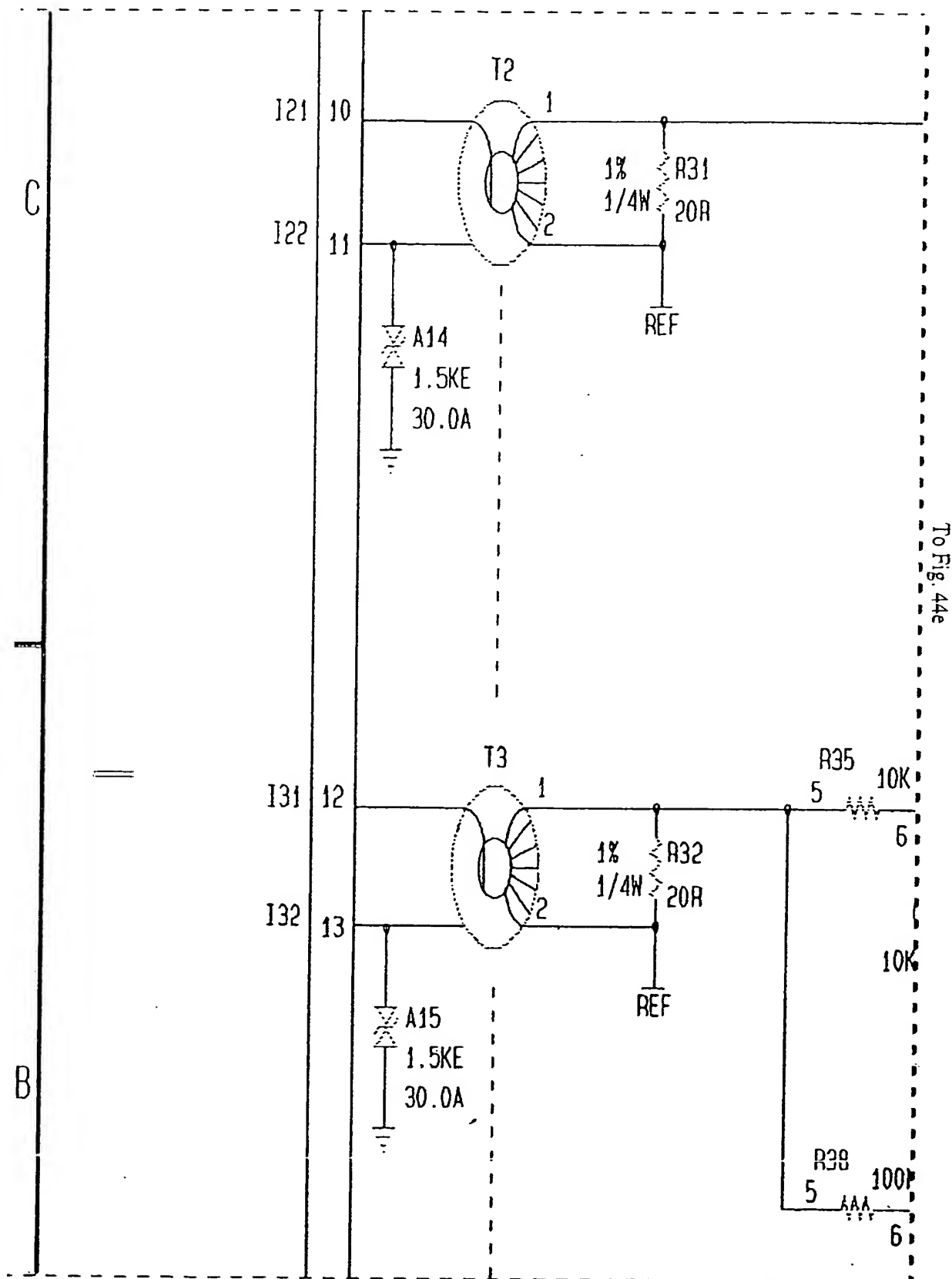
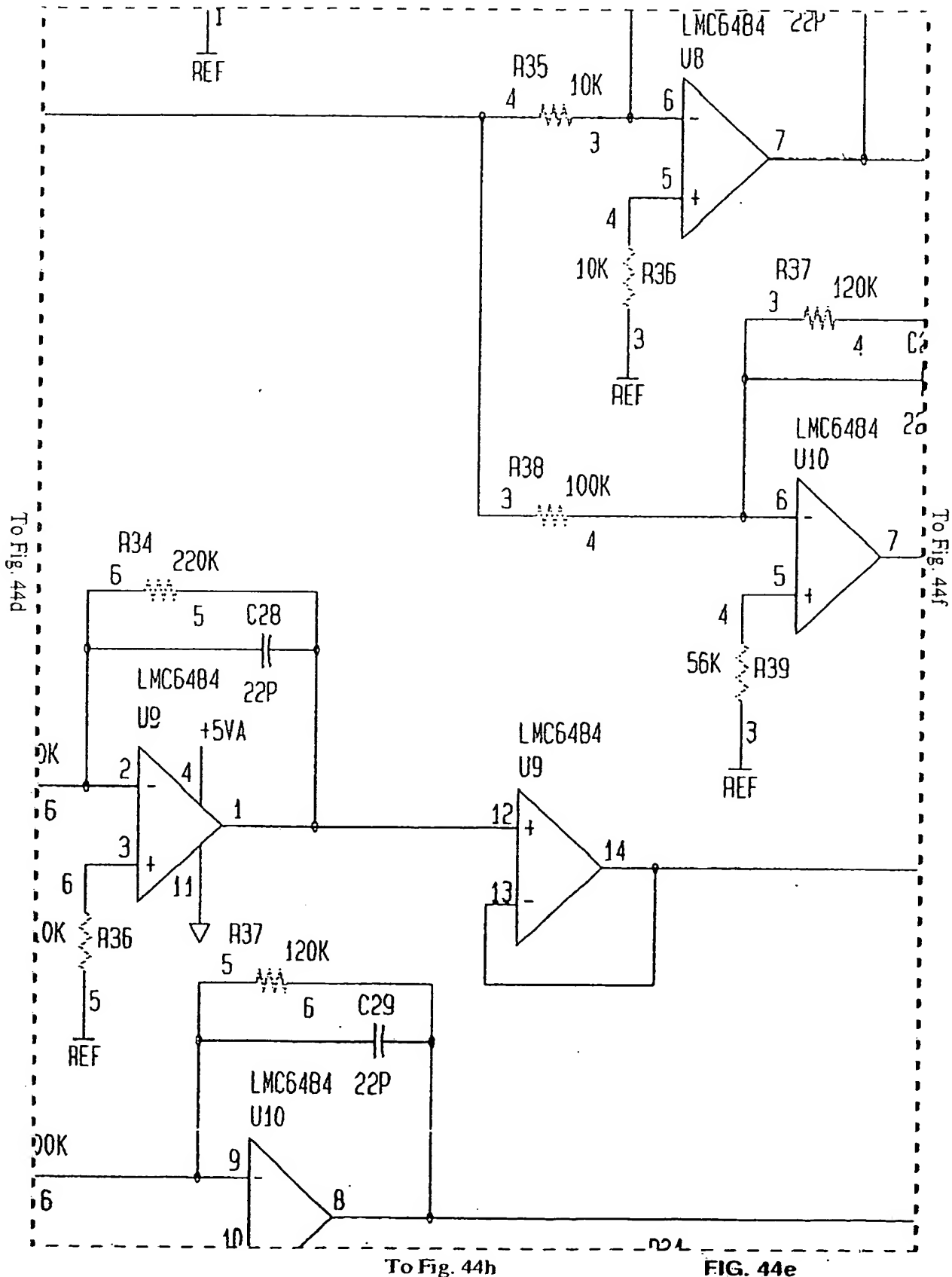


FIG. 44d

To Fig. 44b

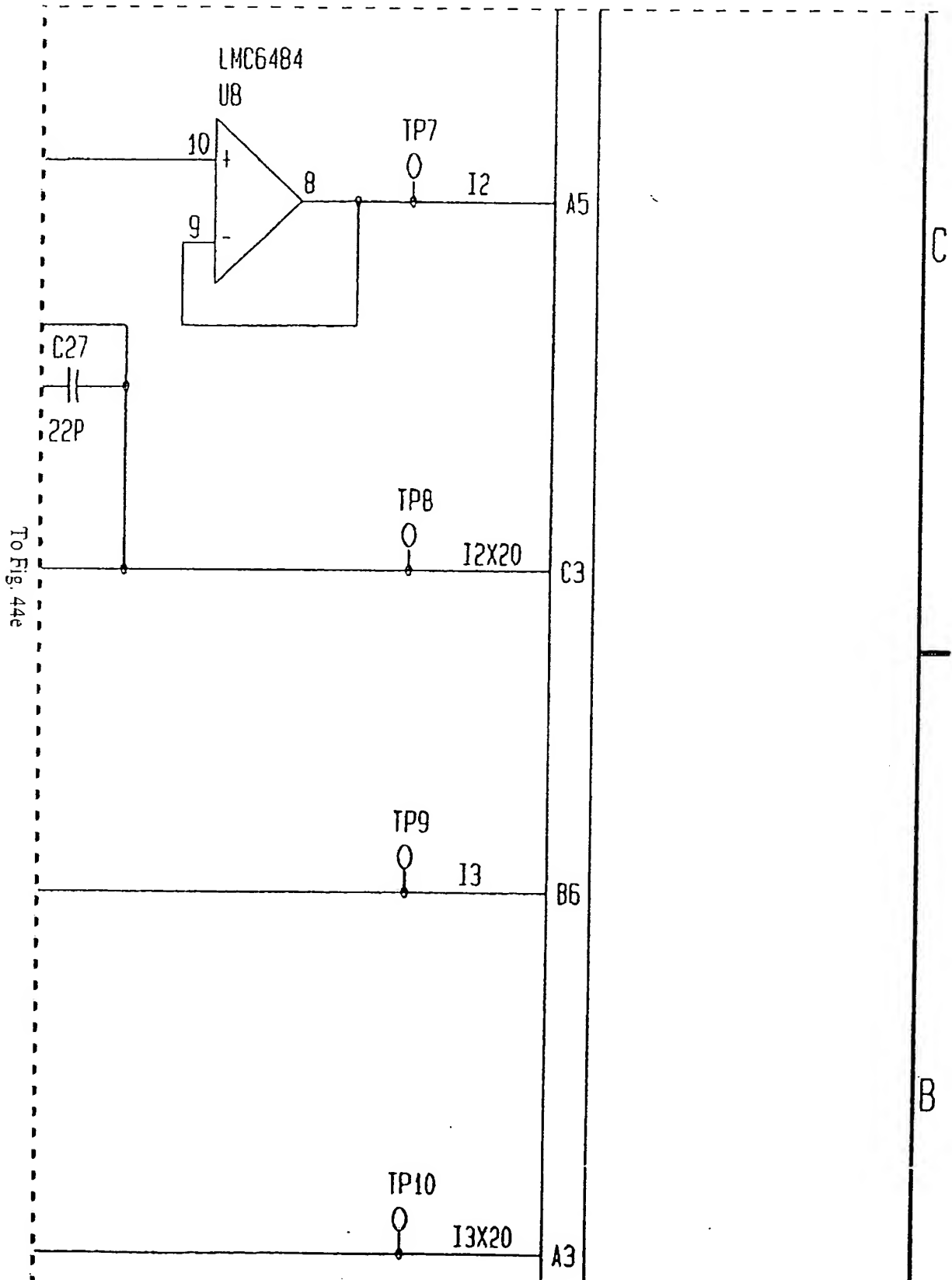


To Fig. 44h

FIG. 44e

186 06 207

To Fig. 44c



To Fig. 44i

FIG. 44f

187 02 207

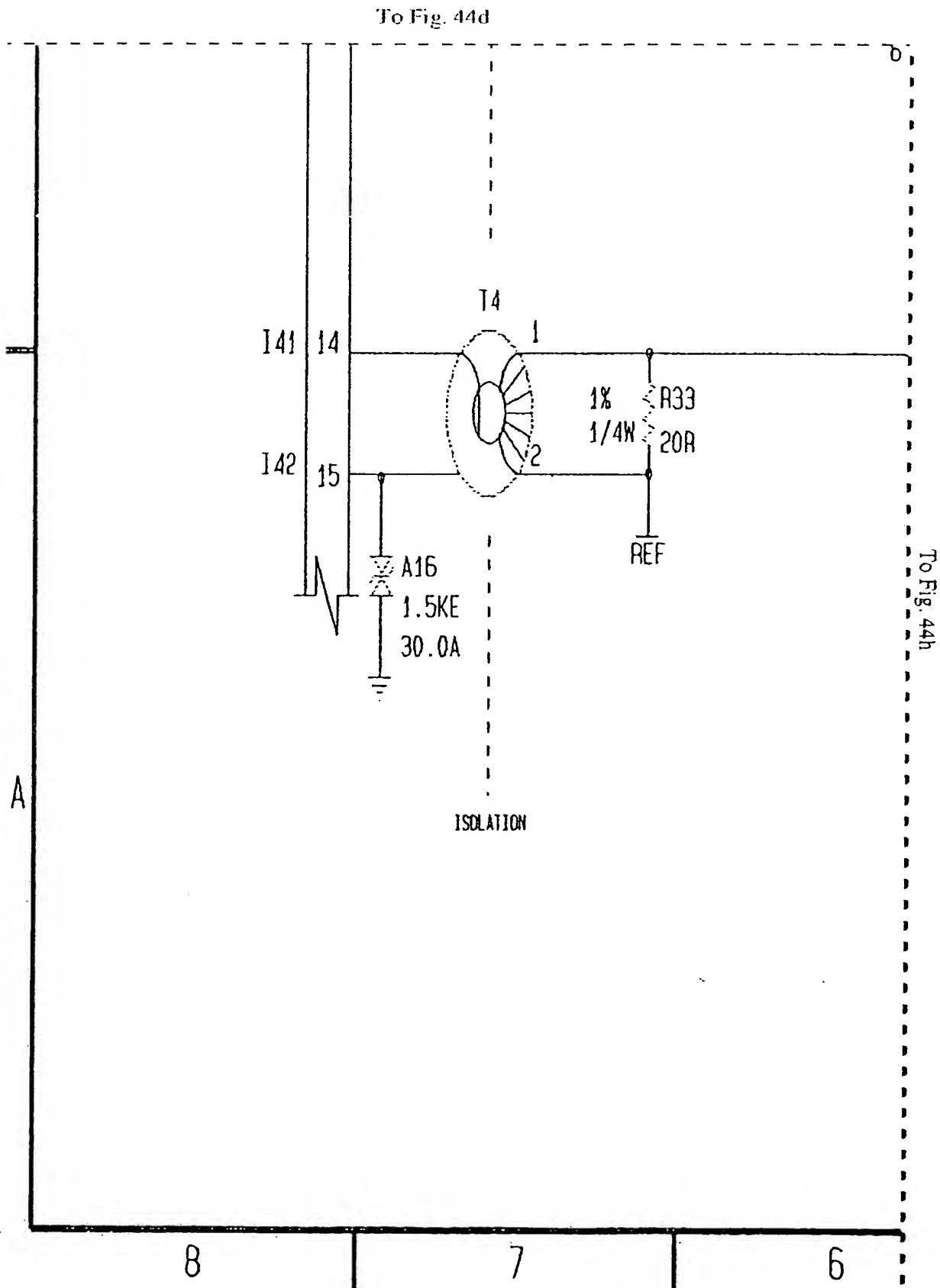


FIG. 44g

180 07 207

To Fig. 44e

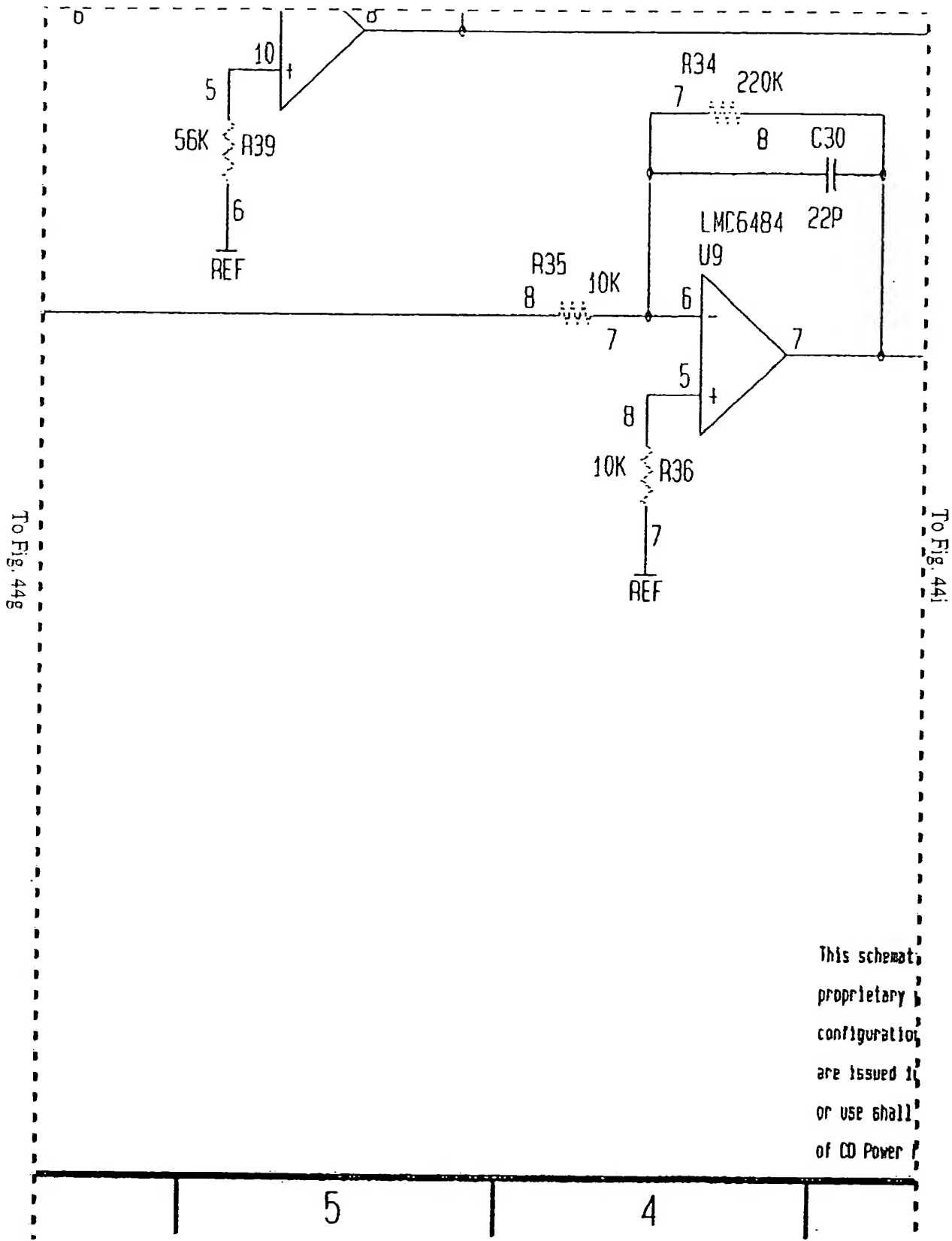


FIG. 44h



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To Fig. 44h



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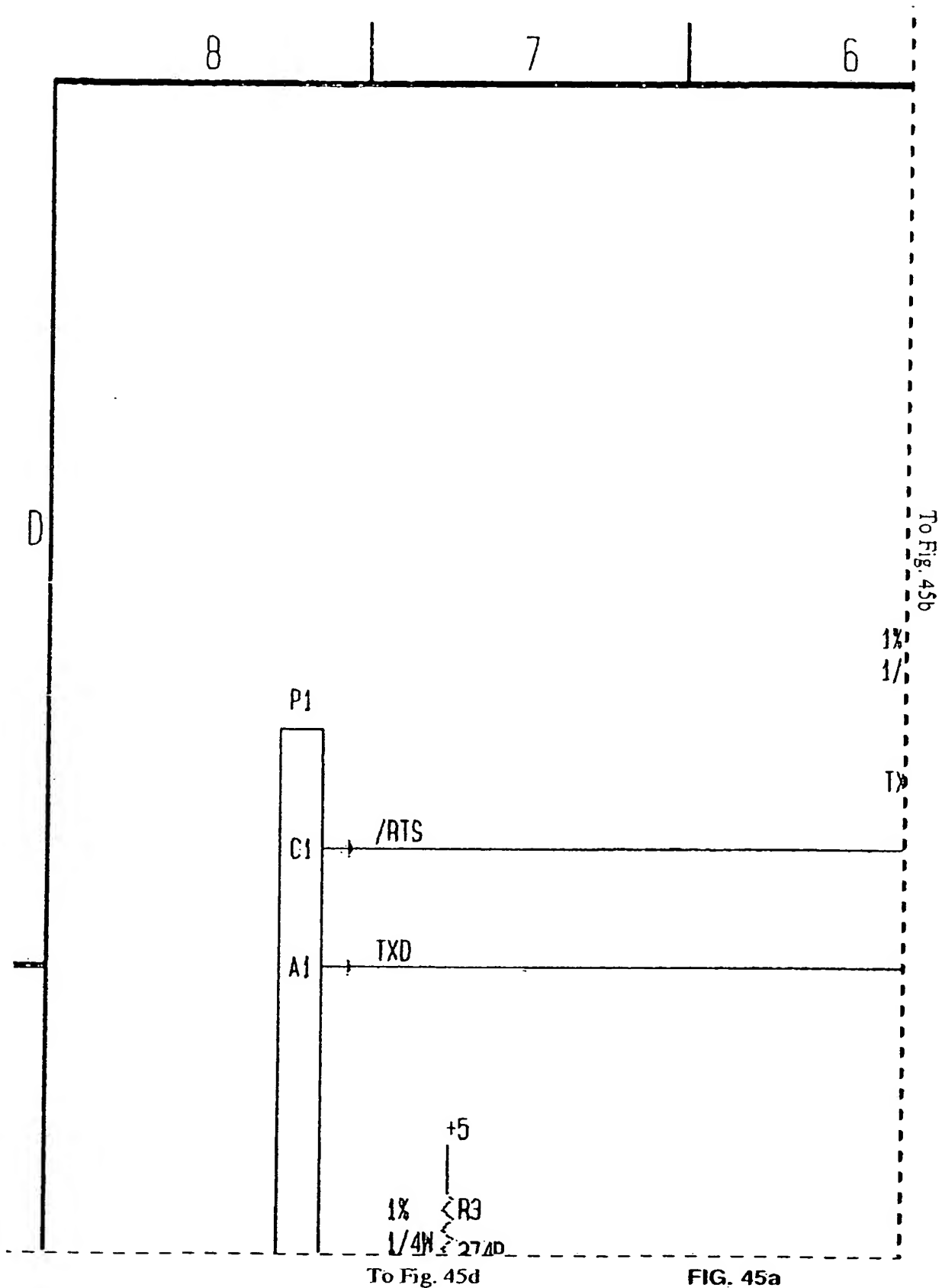
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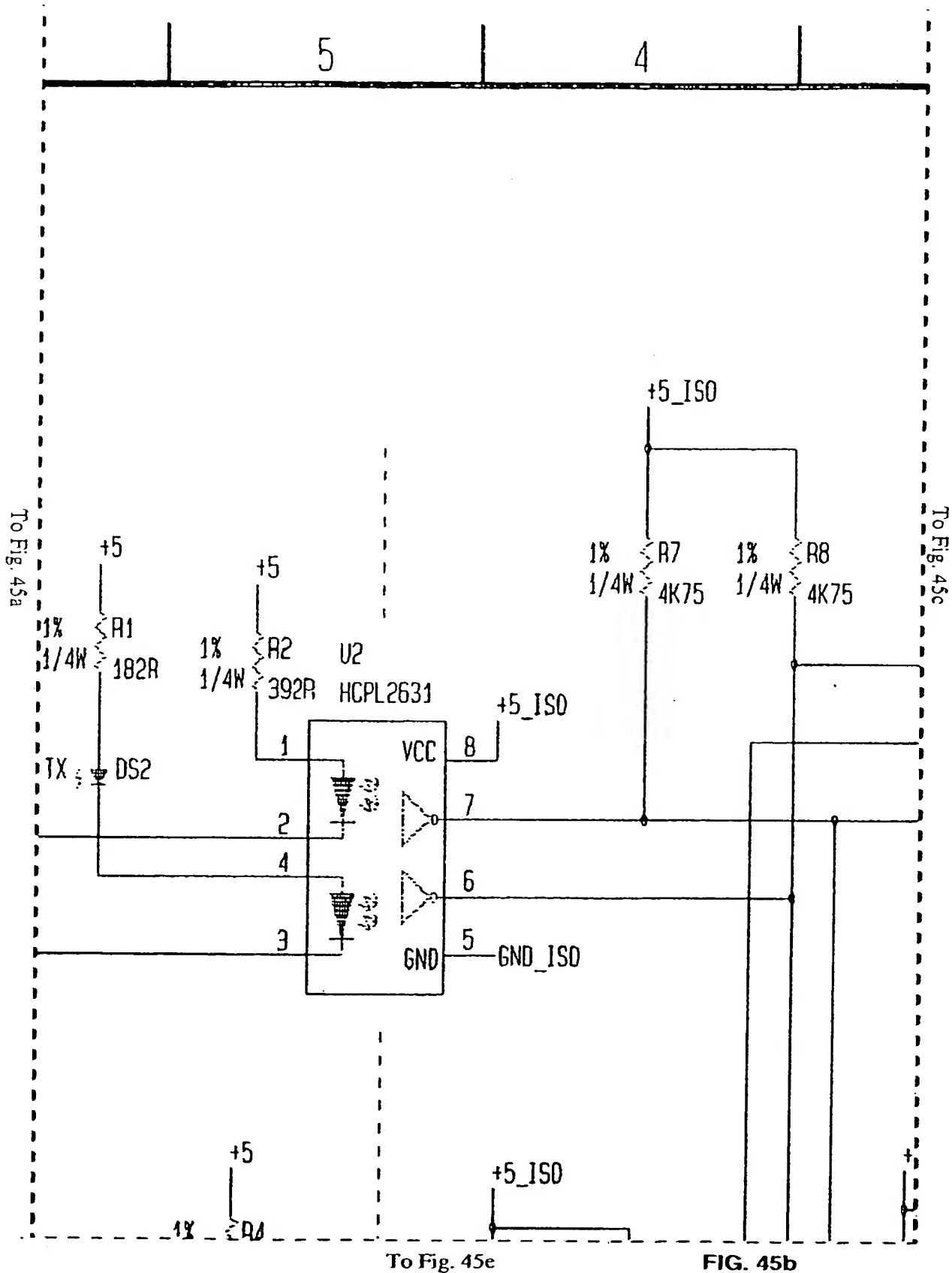
2.

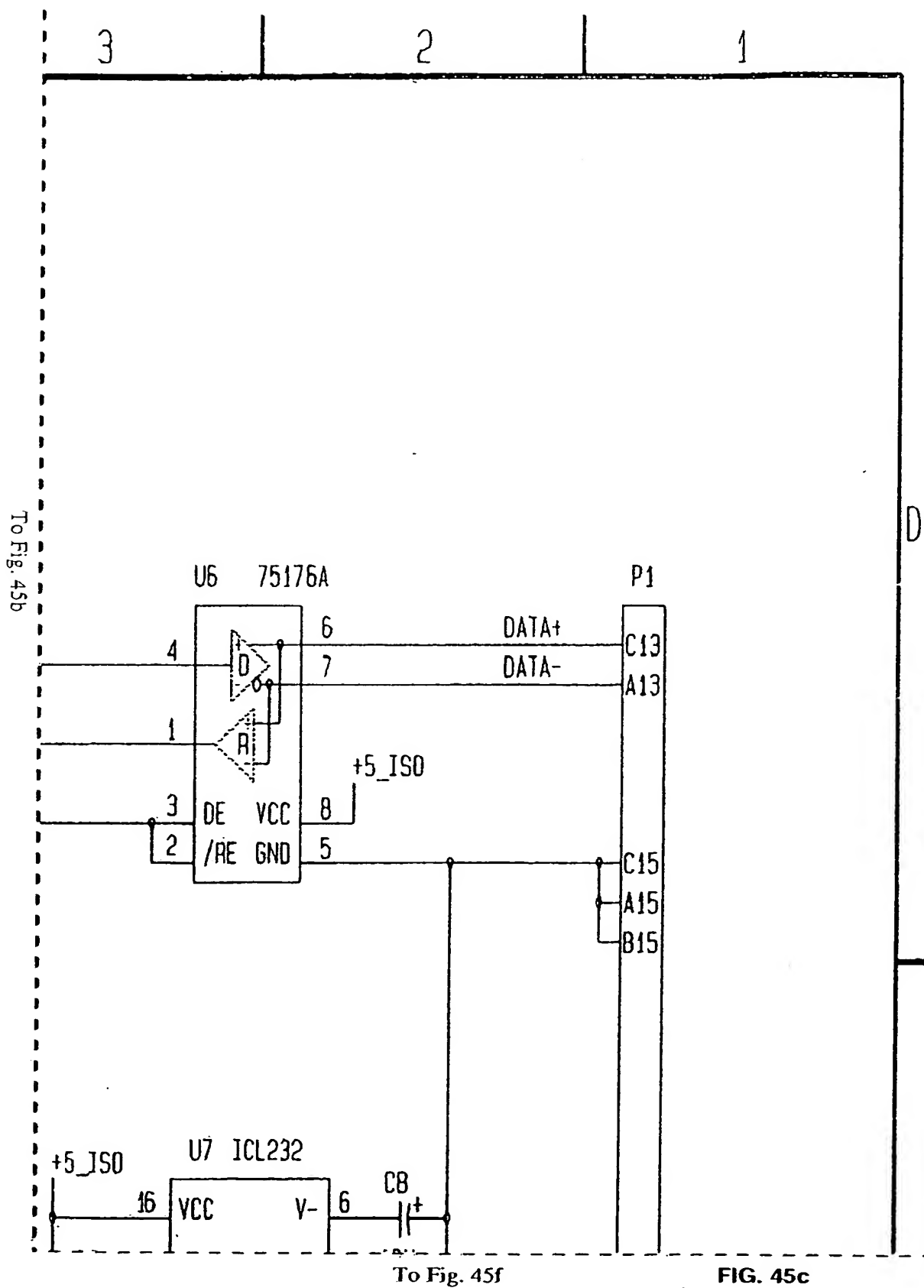
1

**FIG. 44i**

190 07 207

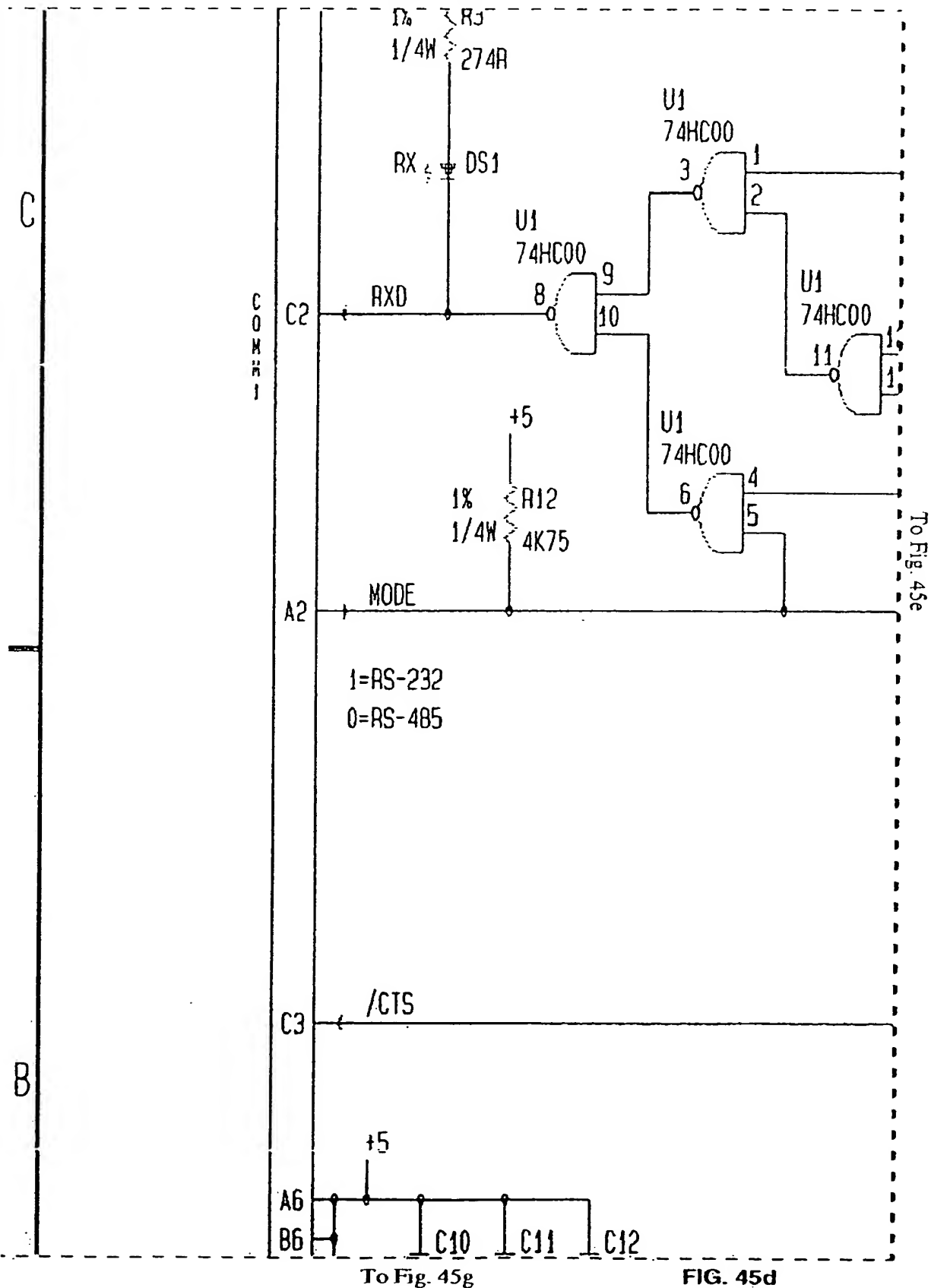






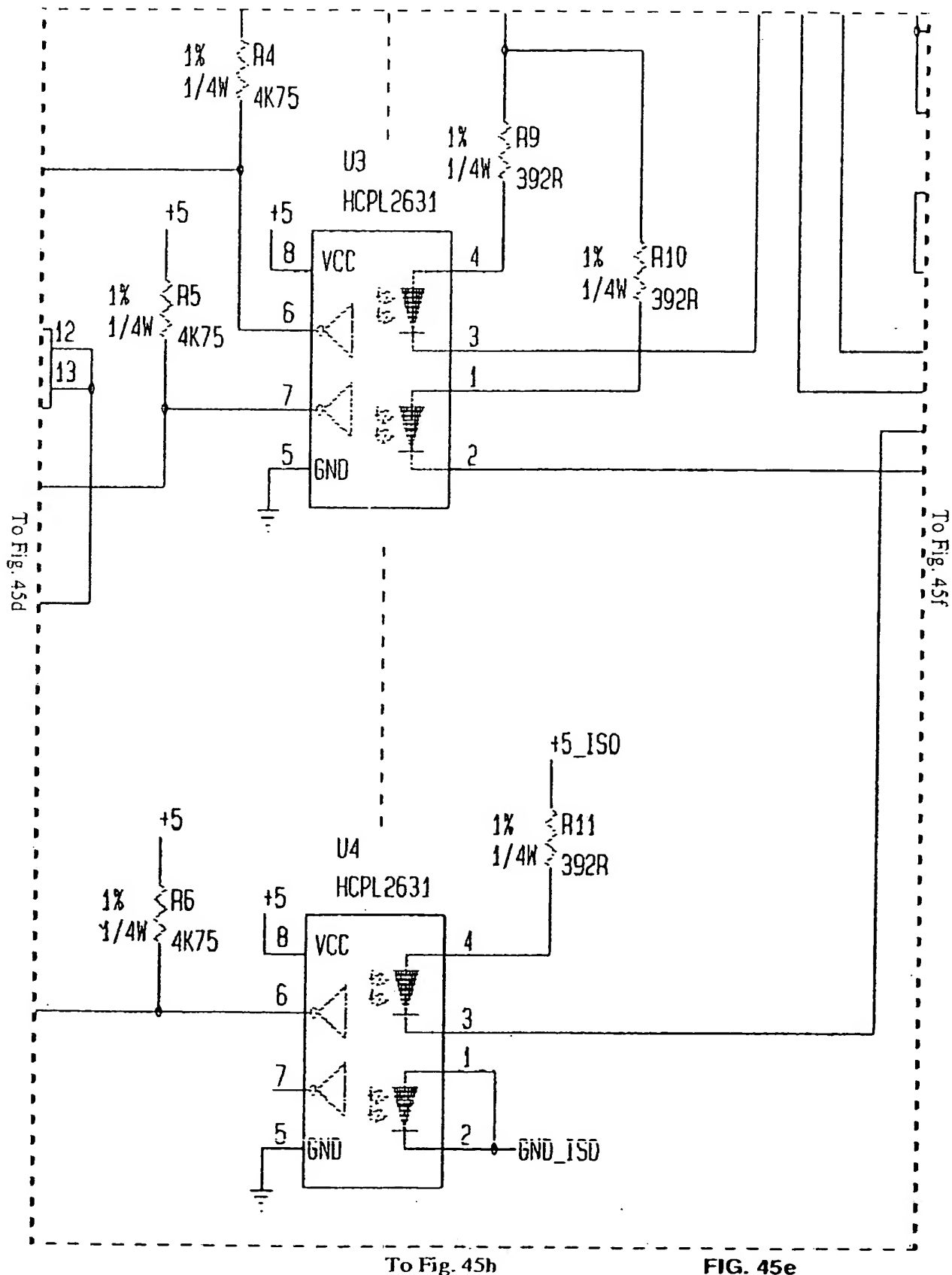
143 07 207

To Fig. 45a



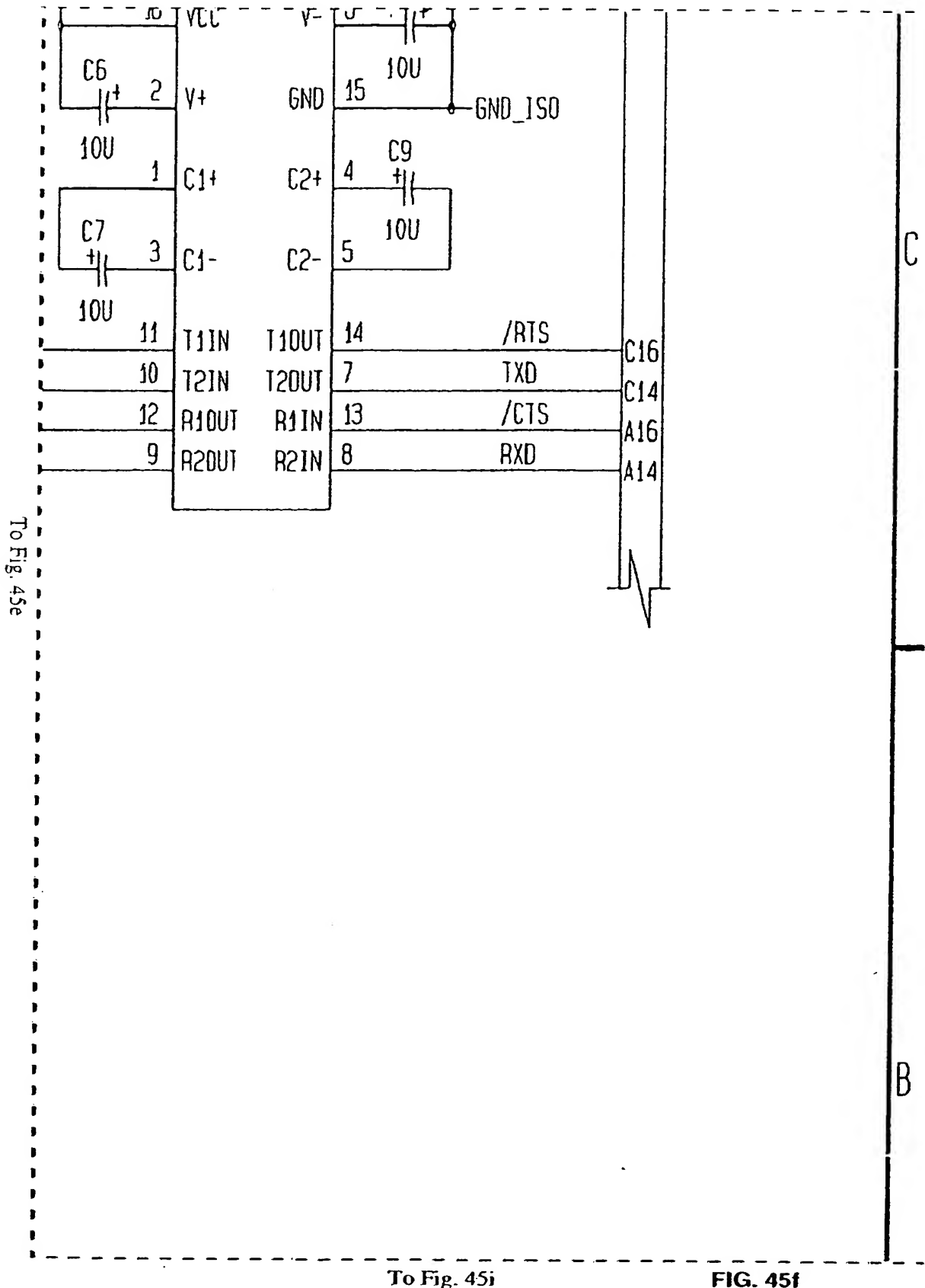
194 56 207

To Fig. 45b



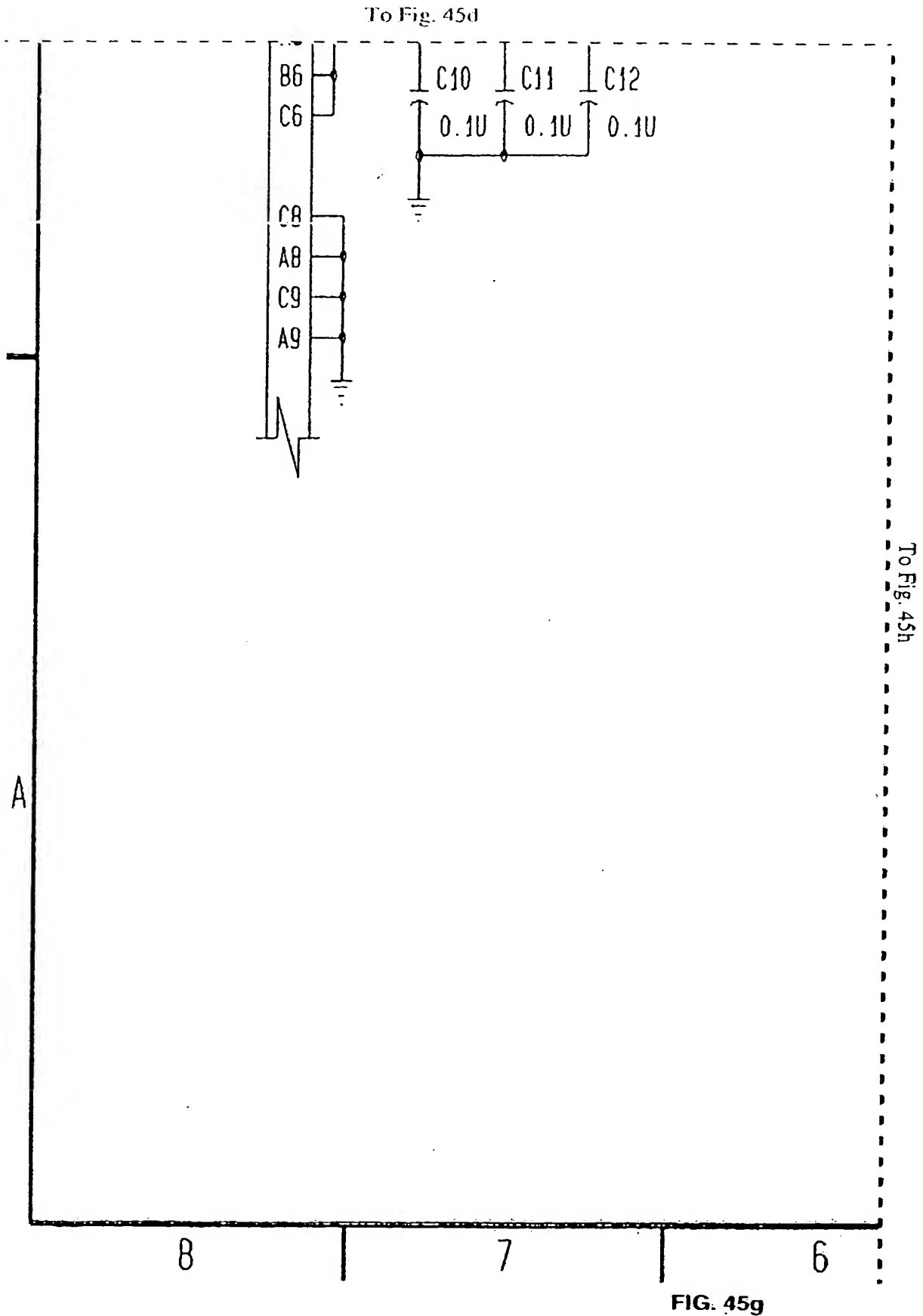
To Fig. 45h

To Fig. 45c



To Fig. 45i

FIG. 45f



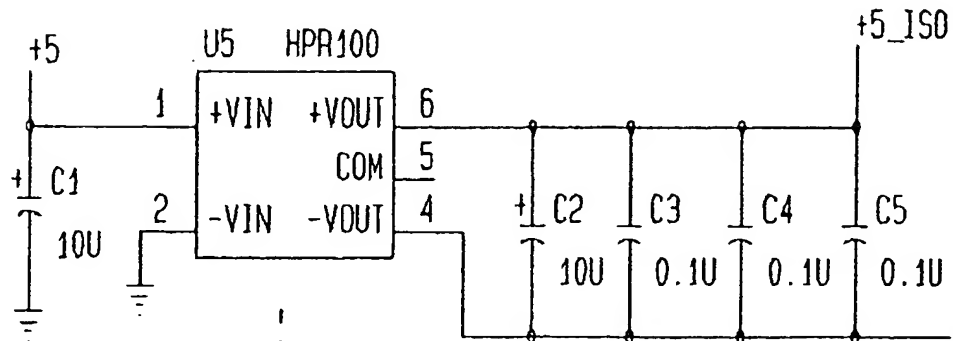


Inventor(s): Ronald G. Hart

Attorney Docket No. 627076, Serial No. 10/068,431

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To Fig. 45c



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198 08 307

To Fig. 45f

To Fig. 45h

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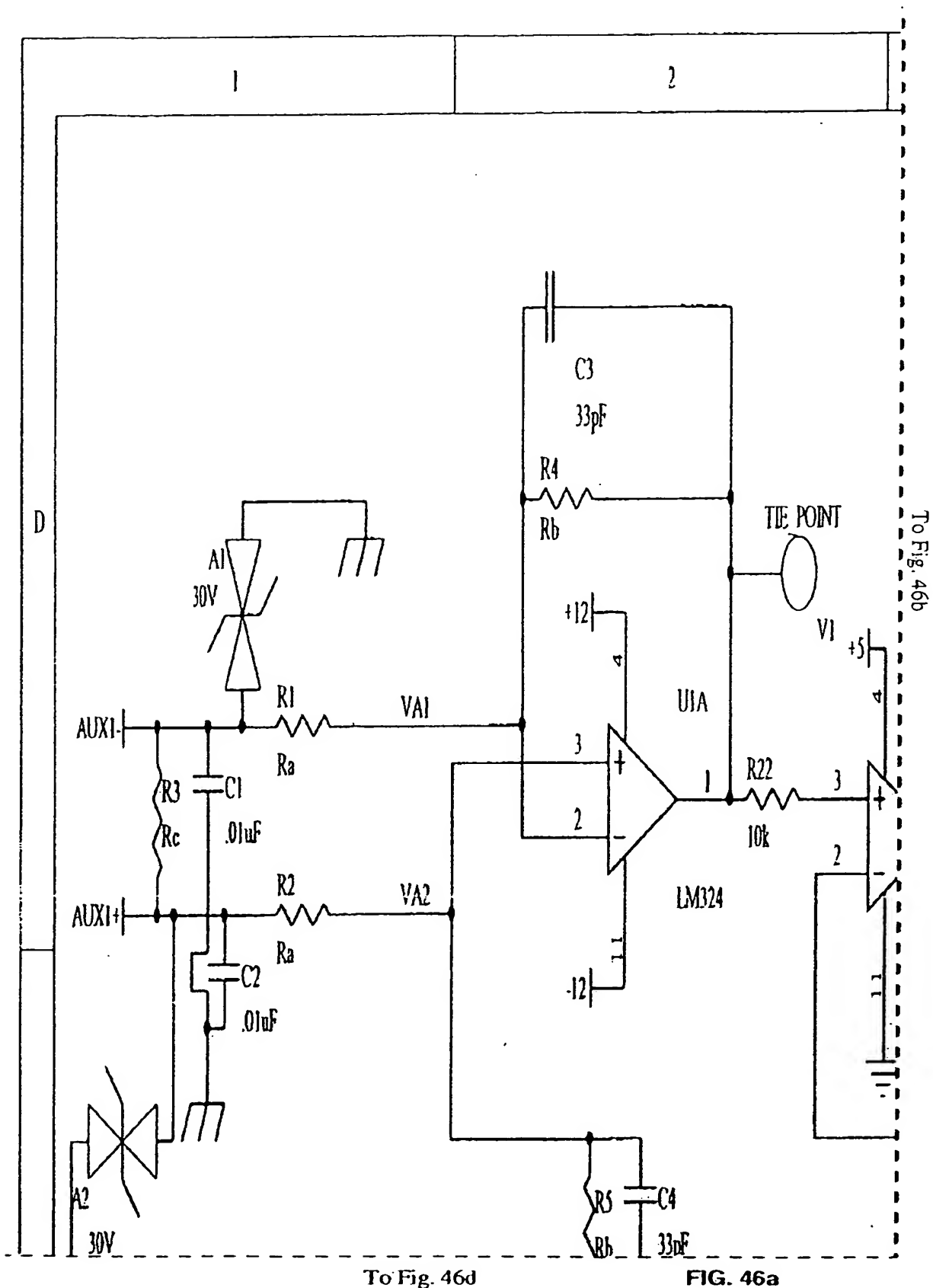
3

2

1

FIG. 45i

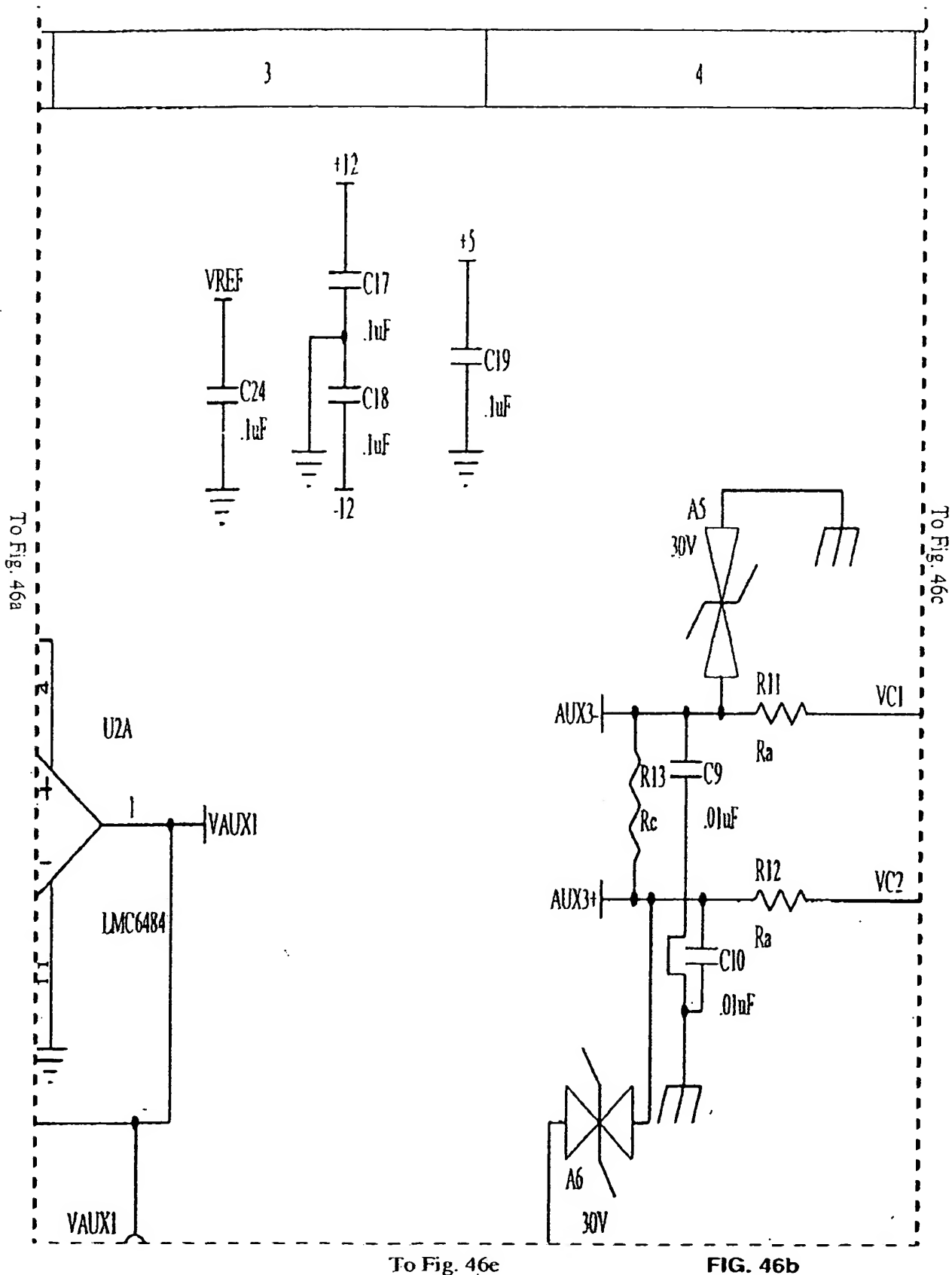
199 08 207



To Fig. 46d

FIG. 46a

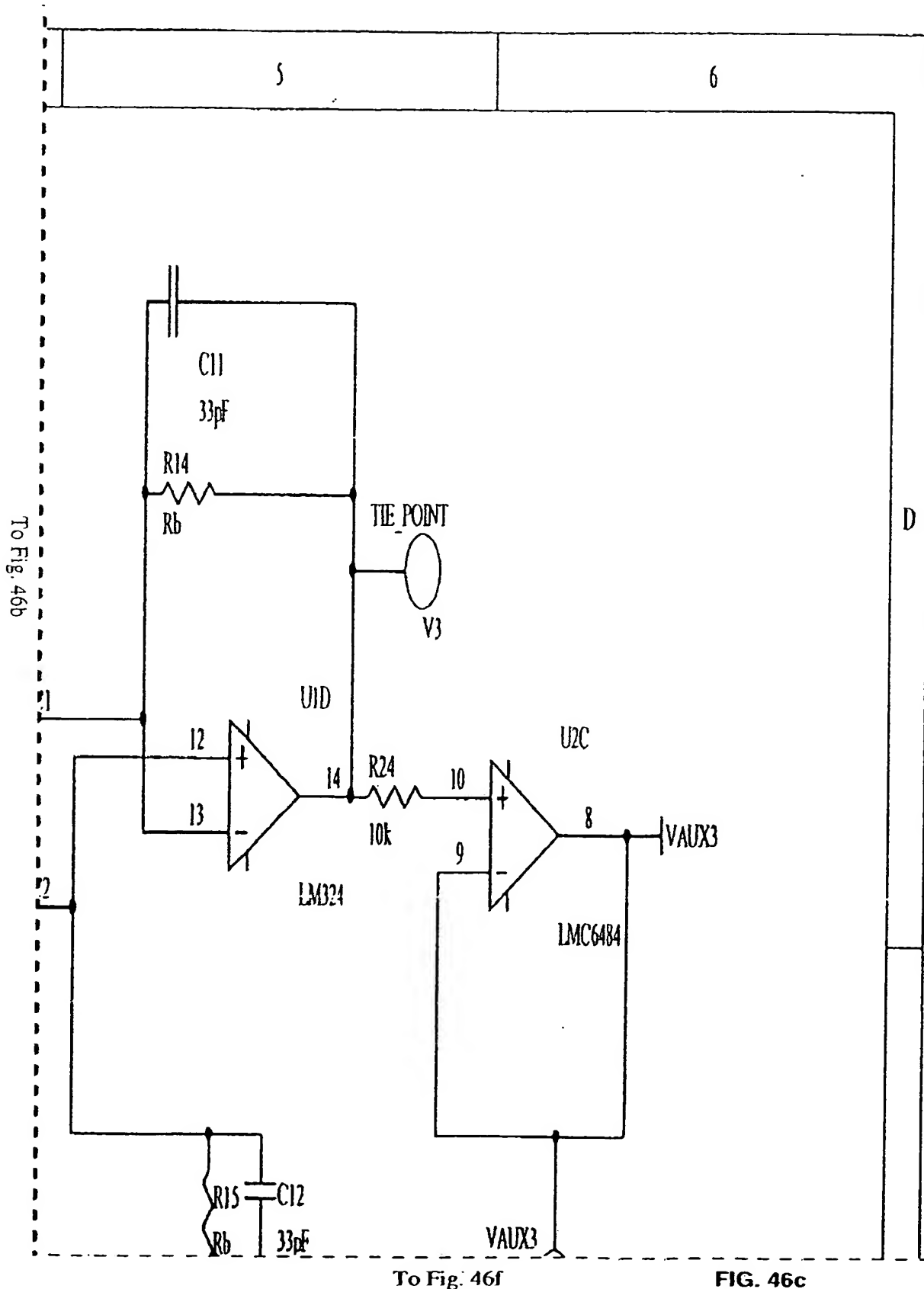
200 8 207



To Fig. 46e

FIG. 46b

201 26 207

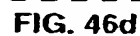


To Fig. 46f

FIG. 46c

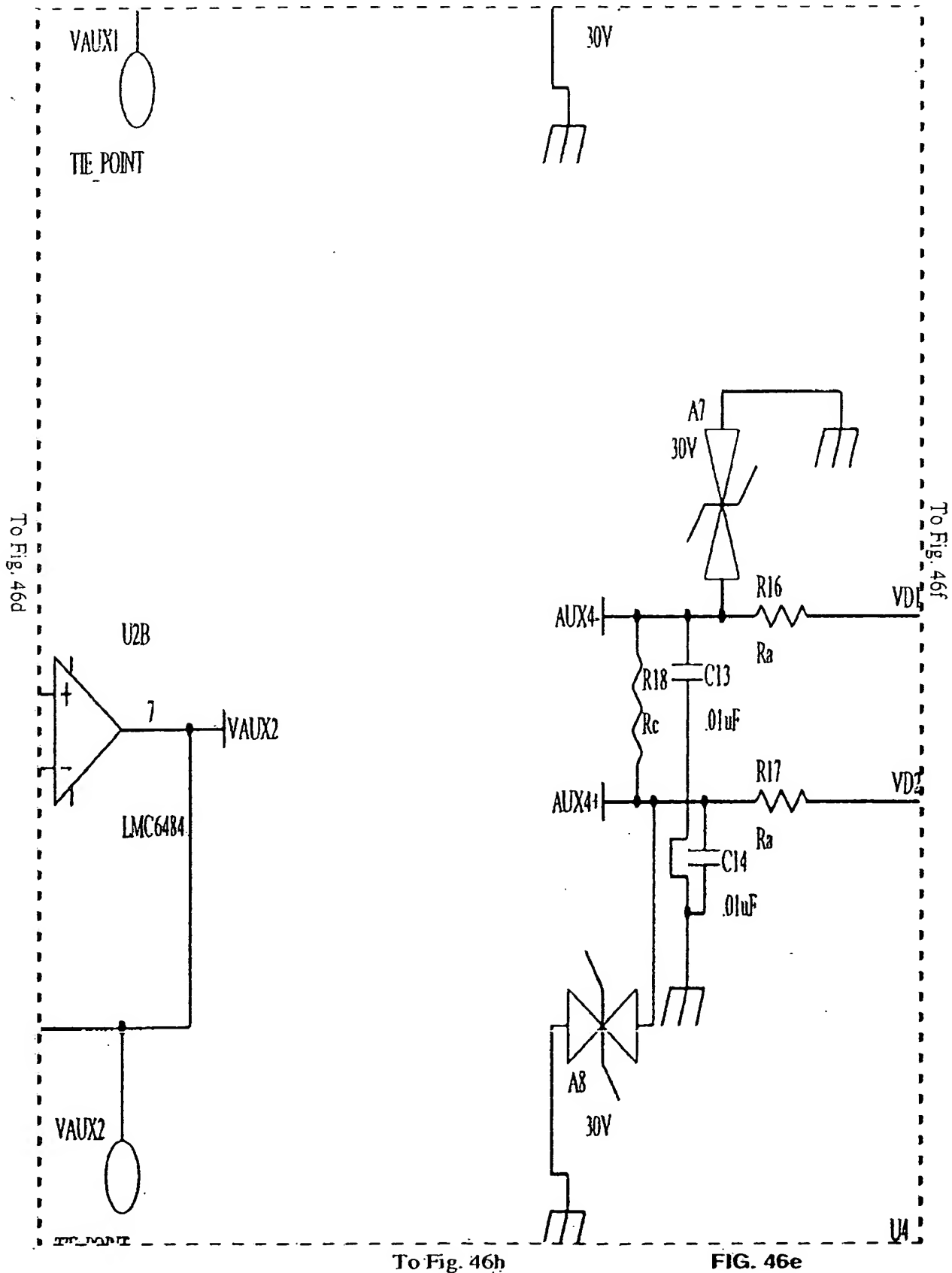
Attorney Docket No. 6270/76, Serial No. 10/068,431

To Fig. 46g



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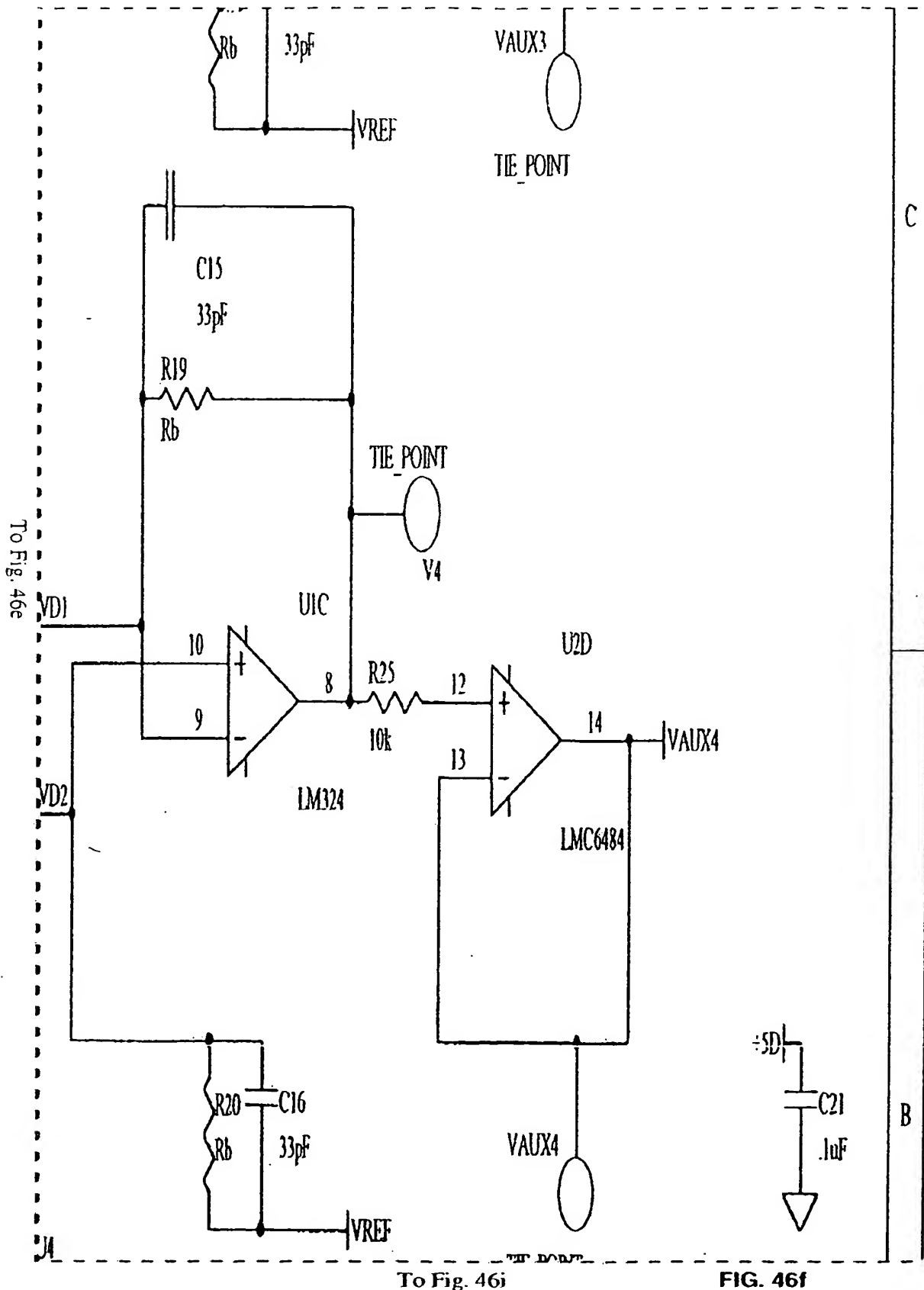
To Fig. 46b



To Fig. 46b

FIG. 46e

To Fig. 46c



To Fig. 46i

FIG. 46f



To Fig. 46d

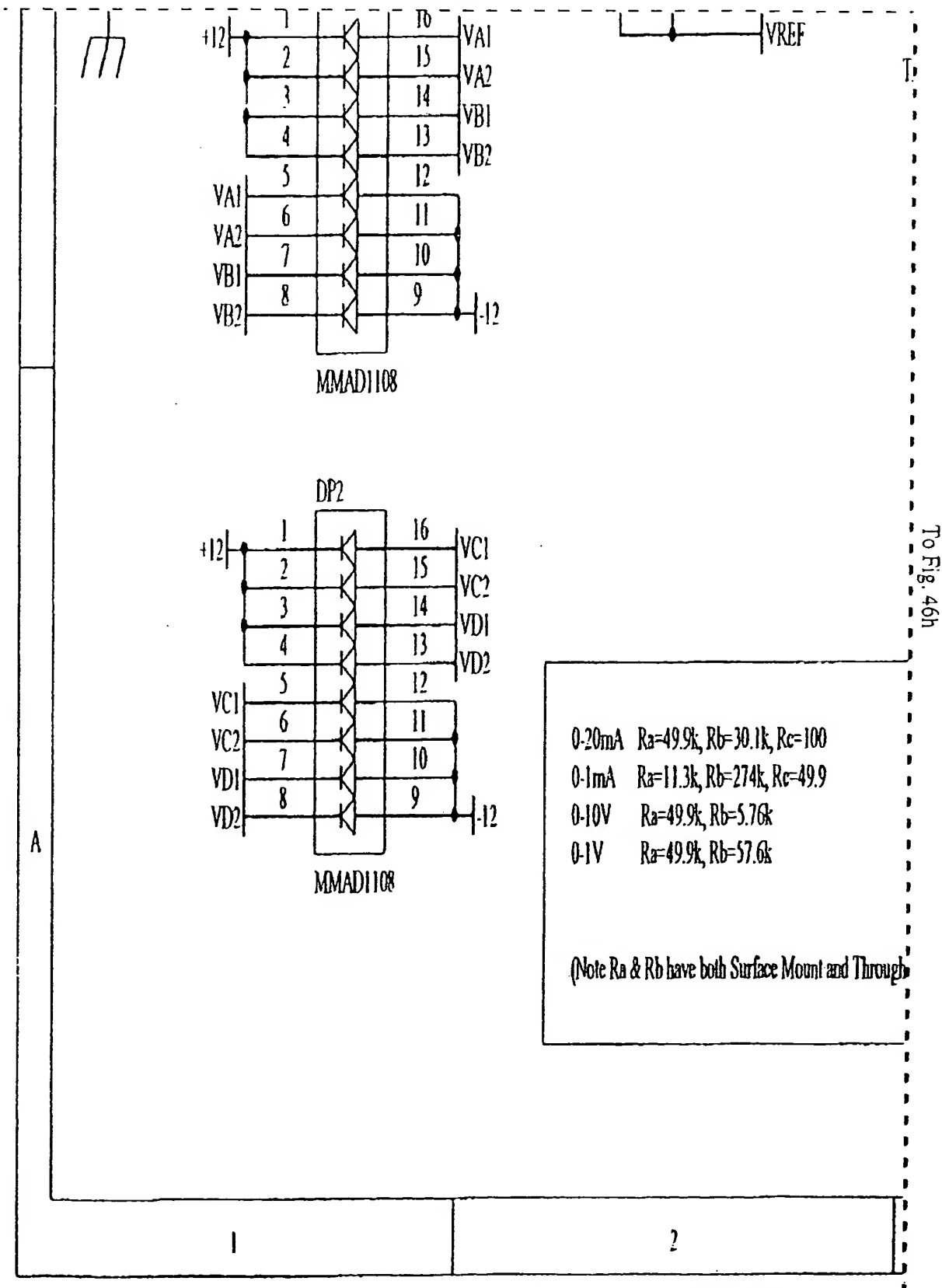


FIG. 46g

To Fig. 46e

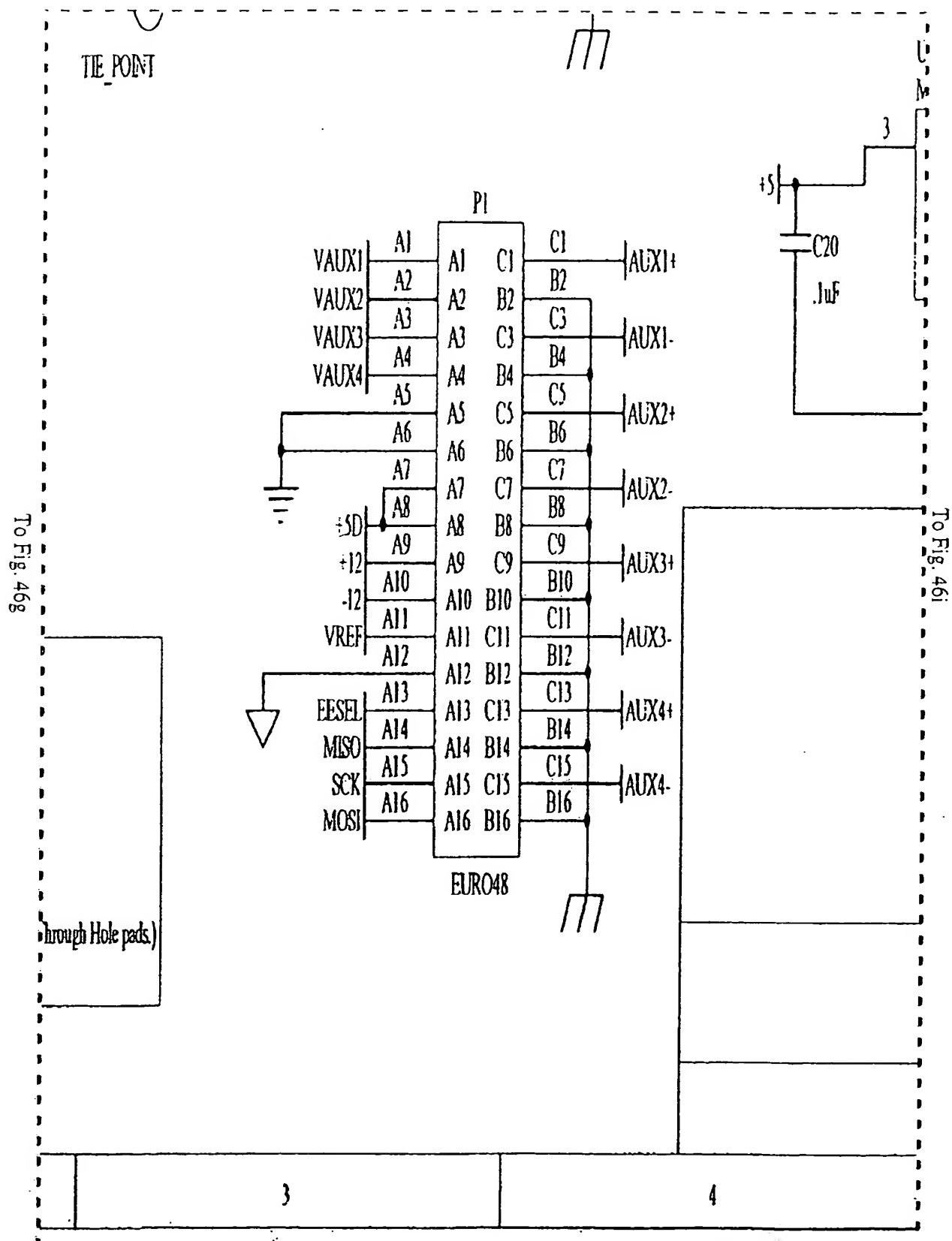


FIG. 46h

To Fig. 46f

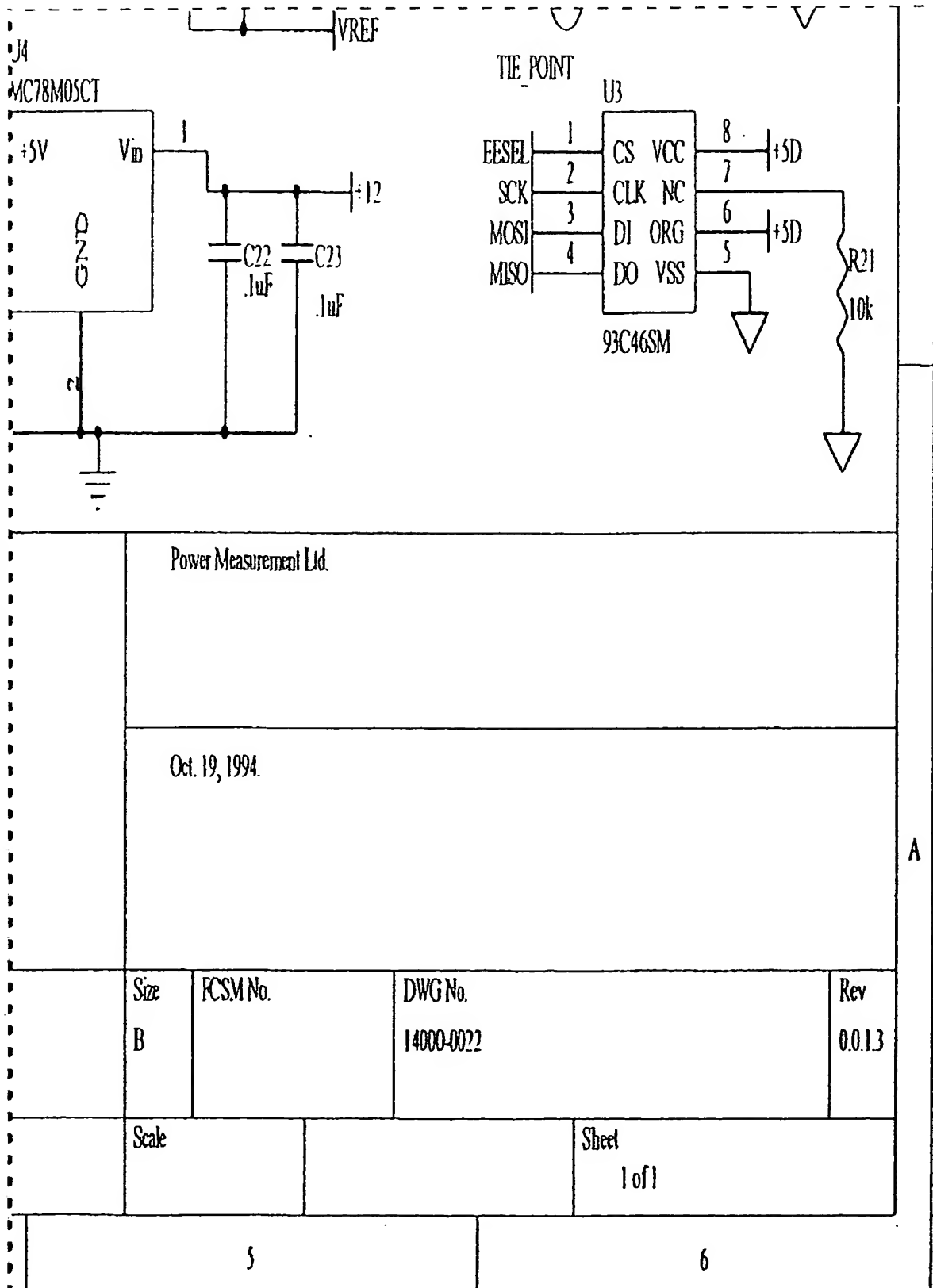


FIG. 46i